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Vertical integration of superconducting solid state coolers

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Vertical integration of superconducting solid state coolers

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ABSTRACT OF THE
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Solid state coolers based on superconducting tunnel junctions are promising low-temperature cooling devices which are routinely fabricated using modern microfabrication methods. Arising applications from quantum technologies often depend on subKelvin temperature to operate, requiring the use of bulky and expensive dilution refrigerators. Solid state coolers can potentially replace dilution refrigerators by cascading several microcoolers operating in different temperature ranges. In order to achieve this, coolers have to be packed efficiently, thus 3D integration is essential. In this thesis, vertical integration of superconducting solid state coolers is studied and developed. Flip-chip bonding is utilized to interconnect two microchips together. Samples are studied before and after bonding, and the thermal resistance of 3D integrated device is determined. Quality assurance of the process focuses on indium bumps and isolation etching of adjacent islands in the cooler device. Cooling is not observed in the device, as the flaws in the isolation etching limit the full capability of the device. However, thermal response of a device is studied, finding that the thermal resistance is significantly improved compared to previous work.

Keywords: superconducting tunnel junction, flip-chip, 3D integration, thermal resistance

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Suprajohtaviin tunneliliitoksiin perustuvat kiinteän olomuodon jäähdyttimet ovat lupaavia matalien lämpötilojen jäähdytyslaitteita, joita valmistetaan rutiininomaisesti moderneilla mikrotuotanto menetelmillä. Uudet kvanttiteknologian sovellukset toimivat yleensä alle Kelvinin lämpötiloissa, joka vaatii isojen ja kalliiden laimennusjäähdyttimien käyttöä. Kiinteän olomuodon jäähdyttimet voivat mahdollisesti korvata laimennusjäähdyttimet ketjuttamalla eri lämpötila-alueilla toimivia mikrojäähdyttimiä. Tämän saavuttamiseksi, jäähdyttimet tulee pakata tehokkaasti, joten 3D integraatio on välttämätöntä.

Tässä tutkielmassa tutkitaan ja kehitetään suprajohtavien kiinteän olomuodon jäähdyttimien päällekkäistä integraatiota. Flip-chip liitostekniikkaa hyödynnetään kahden mikrosirun liittämisessä toisiinsa. Näytteitä tutkitaan ennen ja jälkeen liitoksen, sekä määritetään 3D integroidun laitteen lämpöresistanssi. Valmistusprosessin laadunvarmistus keskittyy indium nystyihin ja vierekkäisten saartojen eristyssyövytykseen jäähdytinlaitteessa. Laitteessa ei havaita jäähdytystä, sillä vajaa eristyssyövytys rajoittaa laitteen täyttä toimintaa. Laitteen suorituskykyä tutkitaan lämpöresistanssin osalta, ja se määritetään edellistä tutkimusta huomattavasti paremmaksi.

Avainsanat: suprajohtava tunneliliitos, flip-chip-liitos, 3D integraatio, lämpövastus

Preface

This thesis was produced at VTT Technical Research Centre of Finland Ltd, working in Nanosystems team and microcooler project from 1/2021 to 6/2021. I'd like to thank my team leader Sanna Arpiainen for giving me this opportunity and Alberto Ronzani for instructing the work already from 6/2020 when I first started at VTT. I also thank especially Janne Lehtinen for all the help regarding the fabrication, characterization, and everything in between. Additionally I show gratitude for the rest of the microcooler team: Antti Kemppinen, Emma Mykkänen, Mika Prunnila and Lassi Lehtisyrjä. It's been pleasure to work with such a great people. I thank Jukka Pekola from Aalto University for supervising the thesis.

A lot was done throughout the spring 2021 for the thesis and other projects, and I'd like to thank the extensive amount of people who I enjoyed to work with in the cleanroom, the low-temperature laboratory and the office: Jaakko Salonen, Leif Grönberg, Sophie Chevalliez, Debopam Datta, Visa Vesterinen, Elsa Mannila, Prometheus DasMahapatra, Sayani Majumdar, Anton Murros, Tarusisko Hirvenoja, Kestutis Grigoras, Ali Shah, Jaana Marles, Jonna Piiroinen and Päivikki Repo.

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Despite of unexpected setbacks and delays ranging from home quarantine to measurement infrastructure problems, the thesis was completed successfully on time. The work continues and hopes are high for realization of a 3D integrated solid state microcooler.

Espoo, 5.7.2021

Joel Hätinen

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1 Introduction

Development of quantum technologies has been remarkable in the recent years. In 1900, Max Planck hypothesized that an electromagnetic radiation would need to be quantized in order to explain the black-body radiation and solve the ultraviolet catastrophe. Followed by Einstein's explanation for photoelectric effect, De Broglie's electron wave postulate and Schrödinger's wavefunction formulation, the 1900s saw tremendous efforts and progress in quantum physics which have spread all over the different fields in physics. A wide range of applications are based on quantum theory, including lasers, Global Positioning System (GPS) and even classical computers. Billions of silicon transistors inside the ordinary laptops and mobile phones utilize a band theory developed for semiconductors. These transistors perform *classical* computational operations on bits, which represent boolean values of true and false (or 1 and 0). Instead, in *quantum* computing, the qubits are not only binary, but can represent a superposition of 1 and 0 in addition to the binary values. Extensive resources have been dedicated to quantum computing in the 2000s, and the quantum supremacy was first claimed to be demonstrated by Google in 2019 [1]. Quantum supremacy is the realization of a calculation by a quantum computer in feasible time, which would take impractical amount of time, i.e. hundreds of years, by the classical computer. Presumably, the toughest challenge in building the quantum computer is increasing the coherence time, i.e. the time the qubit holds its quantum state. With superconducting qubits, the coherence time is increased by cooling the microchips near the absolute zero, to tens of milliKelvins or lower. Currently, the only technology able to achieve that, is a dilution refrigerator which circulates a mixture of ^{3}He/^{4}He and provides cooling by the heat of mixing of helium-3 and helium-4. Dilution refrigerators require a large infrastructure compared to the actual device to be cooled down. A gas handling system of a typical dilution refrigerator occupies several cubic meters of space. Starting from a room temperature, a pulse tube cooler is often used to cool the system progressively to few Kelvins. The dilution part then cools the sample space further down, even to milliKelvins.

Alternative to the dilution refrigerator, superconducting tunnel junctions have been demonstrated to cool the electronic temperature down from a temperature of Kelvin to subKelvin ranges [2, 3, 4, 5, 6]. Superconducting tunnel junctions rely on quantum mechanical effect of tunneling through a barrier from normal metal to the superconductor. The superconducting energy gap filters the tunneling electrons by energy, allowing only the most energetic electrons to pass the barrier, thus cooling down the normal metal. The best performing junctions have been demonstrated using metals such as copper, but the research in replacing the metal with a doped semiconductor has been improving as well. The main advantage for using doped semiconductor is the ability to mass produce the chips more efficiently than metal junctions, as the semiconductor fabrication methods are well studied and optimized. In order to achieve feasible cooling power for practical uses, multiple junctions have to be integrated as a single cooling device. Single junctions have been demonstrated up to nanowatt cooling powers in hundreds of milliKelvins [7], which is several orders of magnitude away from e.g. dilution refrigerators, which can provide hundreds of

microwatts of cooling power in the same range [8]. Integration has been demonstrated in 2D [9, 10], but an efficient packing would require 3D assembly. The challenge is, however, not only the packing of the junctions, but the thermal management between different regions of the device.

In this thesis, the first steps in the development of vertical integration of superconducting microcoolers are taken. First, theoretical background is given on superconducting tunnel junctions and their applications, followed by discussion on flip-chip technology. Next, the experimental techniques used in the thesis are presented, starting from the fabrication part and concluding with the measurement schemes after introducing the low-temperature methods. Finally, the experimental results are presented. Analysis is given on the quality assurance of flip-chip samples before and after bonding, focusing on the bump characterization. Thermal performance analysis is given for a 3D integrated flip-chip cooler. Actual cooling is not demonstrated in the device discussed, as an important process step of isolation etching is found not to be adequate for the purpose.

2 Background

2.1 Superconducting tunnel junctions

In the quantum mechanical phenomenon of tunneling, a particle overcomes a potential barrier higher than the particle in energy, and propagates from one side to another. In tunnel junctions, the barrier is formed between two electrodes, which allows controlling the rate of electron tunneling by voltage bias. Biasing the junction generates a net flow of electrons through the barrier, leading to a net electric current.

Normal metal-Insulator-Normal metal or NIN junctions use metals in their normal conducting state as electrodes between a thin insulating film acting as the tunneling barrier. Electrons being fermions, thus obeying Pauli's exclusion principle, follow the Fermi-Dirac distribution when occupying the energy levels in a metal. The Fermi-Dirac distribution is given by

$$f(E,T) = \frac{1}{e^{(E-\mu)/k_{\mathrm{B}}T}+1}, \tag{1}$$

where f is the probability to occupy an energy level E at temperature T, μ is the chemical potential and k_{B} is the Boltzmann's constant. Probability as a function of normalized energy is plotted for various thermal energies $k_{\mathrm{B}}T$ in Fig. 1. As the temperature approaches zero, the occupation function converges to a step function, indicating that the energy levels below the Fermi energy are filled, and all above are empty. Increase of the temperature smears the occupation function yielding in particular a high-energy tail, i.e. what we refer to as "hot electrons".

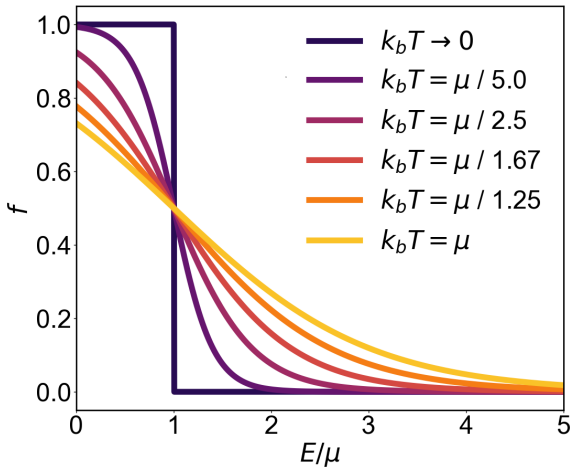

Figure 1: Occupation probability for fermions as a function of energy normalized with the chemical potential for different thermal energies $k_{\mathrm{B}}T$.

NIN junctions being ohmic due to the constant density of states in normal metal, the tunneling current is simply given by

$$I_{\mathrm{NIN}} = G_{\mathrm{NIN}}V, \tag{2}$$

where G_{NIN} is the conductance of the junction and V is the applied bias voltage. Linear current-voltage characteristic of the NIN junction being trivial, the situation changes when one or both electrodes are superconducting. Normal metal-Insulator-Superconductor or NIS junctions operate below the critical temperature of the superconductor. In the superconducting state, an energy gap Δ is opened in the density of states (DOS) of the system. The energy gap is predicted by Bardeen-Cooper-Schrieffer (BCS) theory to form due to a small attraction mediated by the lattice phonons which binds two electrons together, forming a Cooper pair. Cooper pairs carry the supercurrent, an electric current flowing without dissipation in a superconductor. Change from normal metal state or resistive state to a superconducting state is a material specific property and is characterized by a transition temperature called critical temperature T_{C}. At T_{C}, resistivity of the material drastically drops to zero. Below T_{C}, the superconducting energy gap follows an implicit relation given in Eq. 3 and pictured in Fig. 3 below. In the equation, $N(0)$ is the density of states at the Fermi level for electrons on single spin orientation, Ω is the scattering potential near the Fermi energy, $\hbar$ is the reduced Planck's constant and ω_c is the cutoff frequency of phonon interaction. [11]

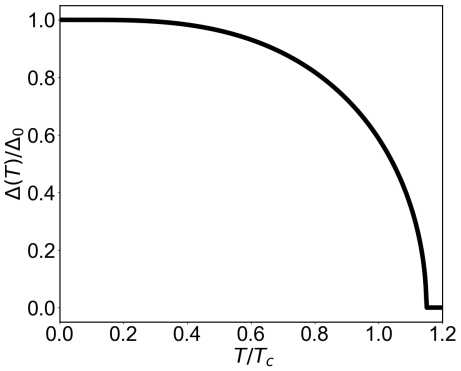

Figure 3. Temperature dependent superconducting energy gap normalized with the zero temperature gap Δ_0 as a function of normalized temperature T/T_{C} .

$$\frac{1}{N(0)\Omega} = \int_{\Delta(T)}^{\hbar\omega_c} \frac{\mathrm{d}E}{\sqrt{E^2 - \Delta(T)^2}} \tanh\left(\frac{E}{2k_{\mathrm{B}}T}\right) \quad (3)$$

Approximation in the weak-coupling limit, where $N(0)\Omega \ll 1$, relates the zero-temperature gap and the critical temperature as [11]

$$\Delta_0 \approx 1.764\, k_{\mathrm{B}} T_{\mathrm{c}}, \quad (4)$$

and temperature dependent gap near the critical temperature as [11]

$$\Delta(T) \approx 1.74\, \Delta_0 (1 - T/T_{\mathrm{c}})^{1/2}. \quad (5)$$

Opening of the superconducting energy gap introduces changes in the density of states available to quasiparticles. In the context of this thesis, quasiparticles are electron-like and hole-like charge carriers in superconductors. The BCS theory yields a normalized density of states as [11]

$$\rho_{\mathrm{BCS}}(E) = \begin{cases} \frac{|E|}{\sqrt{E^2-\Delta^2}}, & |E| > \Delta \\ 0, & \text{otherwise} \end{cases} \tag{6}$$

The BCS density of states holds a discontinuity due to the divergence as $E \to \Delta$. This anomaly is removed in a phenomenological model, Dynes model, which includes an empirical parameter γ, introducing a parametric smearing of the density of states near the energy gap. The Dynes density of states is given as [11]

$$\rho_{\mathrm{Dynes}}(E) = \left| \mathbb{R} \left(\frac{E/\Delta + i\gamma}{\sqrt{(E/\Delta + i\gamma)^2 - 1}} \right) \right|. \tag{7}$$

As $\gamma \to 0$, the density of states converges towards the BCS density of states. Comparison of both density of states is shown in Fig. 2. With non-zero γ, the discontinuity present in the BCS density of states is removed and with increasing γ, the peak at $E = \Delta$ is progressively suppressed.

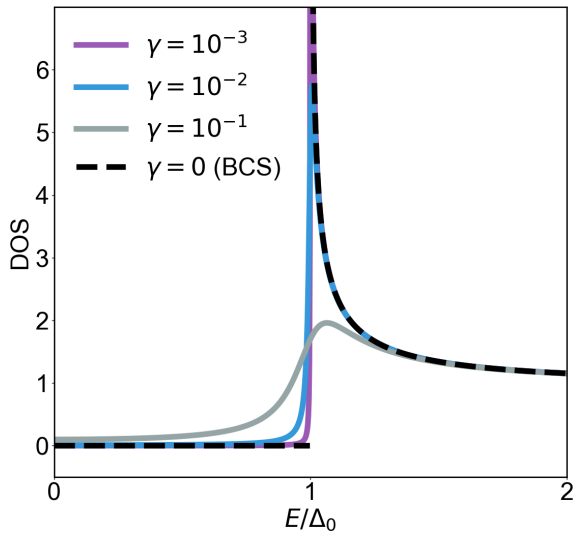

Figure 2: Superconductor density of states as a function of energy normalized with a zero temperature gap with different Dynes γ values and $\gamma = 0$ reducing to the BCS density of states.

NIS junctions utilize the previously discussed properties of superconductors. The quasiparticles tunnel to the available states in superconductor's density of states. The energy dependence of the density of states makes the current-voltage characteristics non-linear. Current in the NIS junction as a function of voltage bias V is given as [11]

$$I_{\mathrm{NIS}} = \frac{1}{eR_{\mathrm{T}}} \int_{-\infty}^{\infty} \rho_{\mathrm{S}}(E)[f_{\mathrm{S}}(E, T_{\mathrm{S,e}}) - f_{\mathrm{N}}(E - eV, T_{\mathrm{N,e}})]\mathrm{d}E, \tag{8}$$

where e is the electron charge, R_{T} is the normal state resistance, E is the energy, ρ_{S} is the normalized density of states of the superconductor (BCS or Dynes), and f_{S} (f_{N}) are the Fermi-Dirac distributions of the superconductor (normal metal). Using the symmetry of the integral and assuming $T_{\mathrm{N,e}} = T_{\mathrm{S,e}}$, the current can be shown to be independent of the electronic temperature at the superconductor side $T_{\mathrm{S,e}}$: [3]

$$I_{\mathrm{NIS}} = \frac{1}{2eR_{\mathrm{T}}} \int_{-\infty}^{\infty} \rho_{\mathrm{S}}(E)[f_{\mathrm{N}}(E - eV, T_{\mathrm{N,e}}) - f_{\mathrm{N}}(E + eV, T_{\mathrm{N,e}})]\mathrm{d}E. \tag{9}$$

Differentiating the current with respect to the voltage gives the differential conductance as [11]

$$G_{\mathrm{NIS}} = \frac{\mathrm{d}I_{\mathrm{NIS}}}{\mathrm{d}V} = \frac{1}{R_{\mathrm{T}}} \int_{-\infty}^{\infty} \rho_{\mathrm{S}}(E) \left[-\frac{\partial f(E + eV, T_{\mathrm{N,e}})}{\partial (eV)} \right] \mathrm{d}E. \tag{10}$$

Letting $T_{\mathrm{N,e}} \to 0$ reduces the term inside the brackets to Dirac delta. This leads to differential conductance being a direct measure of the density of states of the system as [11]

$$G_{\mathrm{NIS}}\Big|_{T_{\mathrm{N,e}} \to 0} = \frac{\rho_{\mathrm{S}}(e|V|)}{R_{\mathrm{T}}}. \tag{11}$$

Electrical transport characteristics as a function of the temperature, based on the numerical calculations of Eq. 9 and Eq. 10, are shown in Fig. 3. In (a), the temperature dependency of the superconducting energy gap is observed from decreasing the temperature from the critical temperature towards zero. At T_{C}, the junction is ohmic and then starts to open the gap until reaching zero-temperature gap. In (b), analogous features are evident and more notably the similarity to the density of states, as in Fig. 2, is seen as the temperature approaches towards zero. Applications of NIS junctions include low-temperature thermometry, refrigeration and calorimetry [2]. The first two are the most relevant in this thesis, and they are discussed next.

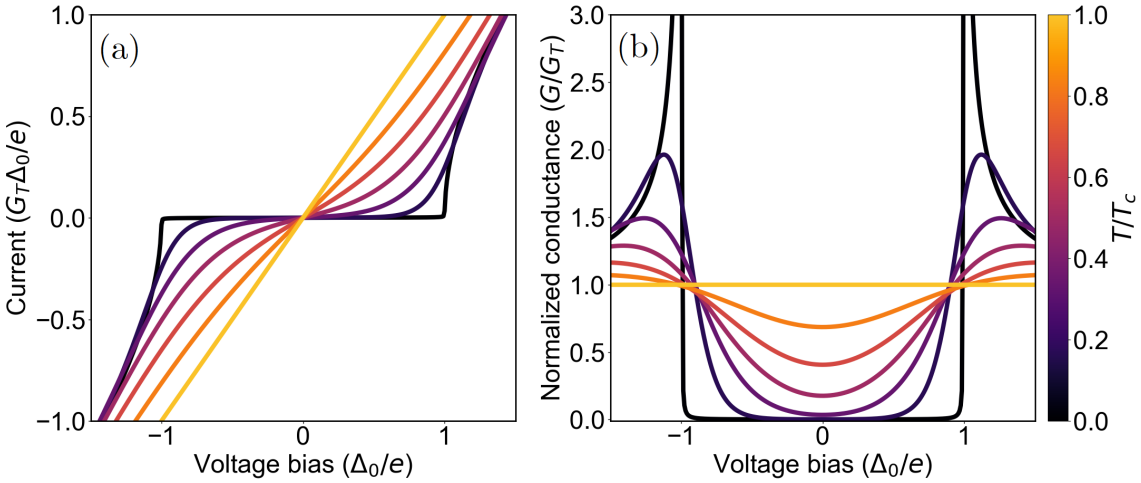

Figure 3: Electrical characteristics of a NIS junction as a function of relative temperature T/T_c. The electronic temperatures in N and S parts are both fixed to T. (a): Current as a function of voltage bias. (b): Normalized differential conductance as a function of voltage bias.

2.1.1 Thermometry

Temperature-dependent tunneling in Kelvin and subKelvin temperature regimes enables low-temperature thermometry. An experimental procedure is to bias the junction with a constant current, sweep the set temperature and record the voltage over the junction. The set up assumes equilibrium between the electron- and phonon temperature in the system. Calibrating this thermometer against a primary thermometer, such as a Coulomb Blockage Thermometer (CBT) [12], allows accurate measurement of the temperature with a single NIS junction. [13] Importantly, NIS thermometers can be easily used directly as an on-chip probes and modern fabrication methods allow creating sub-micrometer sized devices [2]. Figure 4 shows the typical results of (a): current biasing the junction and recording the voltage over the junction, which produces (b): the thermometer curve after calibration. The response of the thermometer generally depends on the Dynes parameter γ, which is set 10^{-3} here for demonstration. Non-zero operation point of the NIS junction induces self-heating of the thermometer. Detrimental effects such as the self-heating is decreased by lowering the bias current as much as possible by other limitations, such as noise in the voltage reading. Another technique is to use a pure AC bias and record the response in a narrow frequency band, see Sect. 3.3.2.

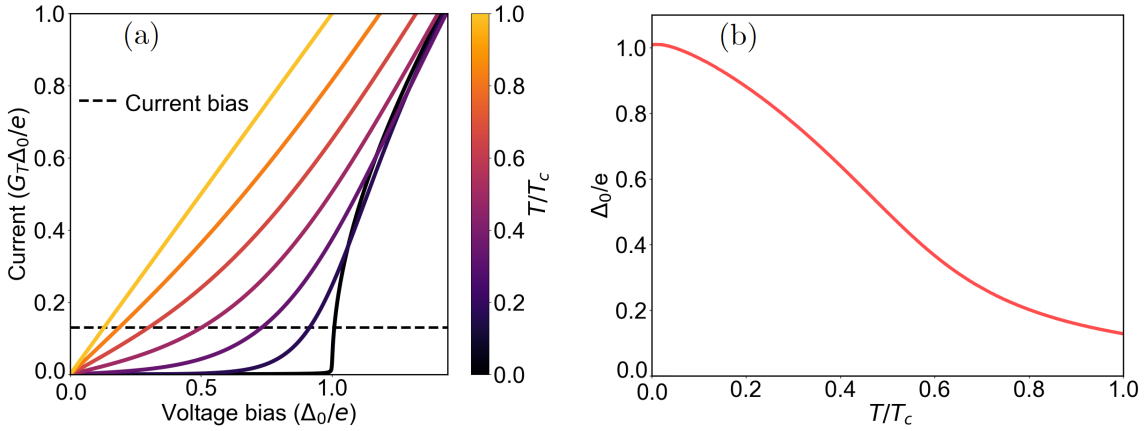

Figure 4: Operation of NIS junction as a low-temperature thermometer. (a): Current-voltage characteristics with a fixed current bias. (b): Voltage over the junction as a function of relative temperature with a fixed current bias and $\gamma = 10^{-3}$.

2.1.2 Refrigeration

NIS junctions have an energy filtering property which enables cooling down the electrons in the normal metal side of the junction relative to the bath temperature. When biased close to the onset of quasiparticle conduction, i.e. at voltage Δ/e, only the most energetic or hottest quasiparticles are able to tunnel through the barrier, resulting in net energy flux, decreasing the temperature of the quasiparticles at the normal metal side. It is good to note that the temperature purely refers to the electronic temperature, and the temperature of the lattice depends also on the coupling between the electron and phonon system. Schematic of the biased NIS junction is shown in Fig. 5(a). The junction is biased with a voltage V which shifts the energy levels of the superconductor such that the lower energy quasiparticles are unable to tunnel from the normal metal to the superconductor due to the gap in the superconductor's density of states. Apart from the above-mentioned ideal case, realistically there is always quasiparticle states inside the superconducting energy gap, described by the Dynes parameter.

Thermal transport power of the NIS junction can be given as [11]

$$P_{\mathrm{NIS}} = \frac{\Delta}{e^2 R_{\mathrm{T}}} \int_{-\infty}^{\infty} (E - eV)\rho_{\mathrm{S}}(E)[f_{\mathrm{S}}(E, T_{\mathrm{S,e}}) - f_{\mathrm{N}}(E - eV, T_{\mathrm{N,e}})]\mathrm{d}E, \tag{12}$$

where $eV \lesssim \Delta$ results in electronic cooling and $eV \gg \Delta$ in Joule heating in the junction. Thermal transport power is calculated in Fig. 5(b) as a function of voltage bias for $\gamma = 10^{-3}$. Real NIS cooler performance can be approximated by assuming a pure BCS density of states (Eq. 6) and quasiequilibrium within T_{N} and T_{S} along with the low-temperature limit $k_{\mathrm{b}}T \ll k_{\mathrm{b}}T_{\mathrm{C}} \approx \Delta_0/1.76$. Then the optimal bias voltage is given as $V_{\mathrm{opt}} \approx (\Delta_0 - 0.66\, k_{\mathrm{b}}T_{\mathrm{N}})/e$, and the maximum cooling power of a single NIS

junction can be approximated as: [3]

$$P_{\mathrm{NIS,\,opt}} \approx \frac{\Delta_0^2}{e^2 R_\mathrm{T}} \left[0.59 \left(\frac{k_\mathrm{b} T_\mathrm{N}}{\Delta_0} \right)^{3/2} - \sqrt{\frac{2\pi k_\mathrm{b} T_\mathrm{S}}{\Delta_0}} e^{-\Delta_0 / k_\mathrm{b} T_\mathrm{S}} \right]. \tag{13}$$

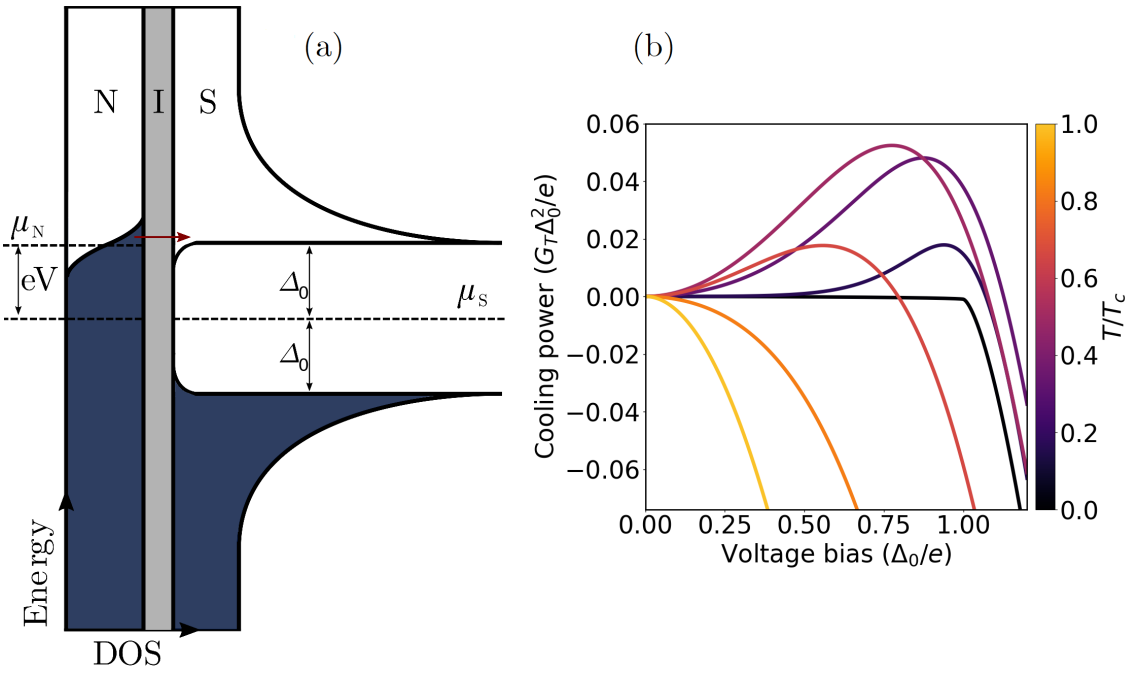

Figure 5: (a): Tunneling in a NIS junction with a voltage bias $V \lesssim \Delta_0$. Fermi level μ_N is shifted with respect to μ_S so that the most energetic electrons are extracted from the normal metal (N) to the superconductor (S) through the tunneling barrier (I). (b): Calculated cooling power in NIS junction as a function of voltage bias with $\gamma = 10^{-3}$. Negative cooling power implies heating power in the junction. The electronic temperatures in N and S parts are both fixed to T.

The most common figure of merit of coolers based on superconducting tunnel junctions is the efficiency

$$\eta = \frac{P_\mathrm{NIS}}{IV} \simeq 0.7 \frac{T_\mathrm{N,e}}{T_\mathrm{c}}, \tag{14}$$

where the second equality applies for an optimally biased cooler in the low-temperature limit. Equation 14 sets the upper limit for the efficiency to around 20% at optimal operation temperature of $T_\mathrm{C}/4$. [2] The efficiency serves as a basic evaluation and optimization parameter for coolers and their design, especially for simple cooler designs utilizing single tunnel junction. Other figures of merit are the maximum temperature difference between the cooler's normal metal and the bath temperature, and the maximum cooling power provided at given temperature. With increasing complexity, for example cascading several cooler stages, the optimization has to be looked in different light. An approximative optimization parameter O can be used

to optimize a cascaded cooler single stage at time: [14]

$$O = \left(\frac{P_{\mathrm{H}} T_{\mathrm{N}}^2}{P_{\mathrm{in}} T_{\mathrm{S}}^2} \right)^{\frac{1}{lg(T_{\mathrm{S}}/T_{\mathrm{N}})}}, \tag{15}$$

where P_{H} is the total heating power to the cooler stage and P_{in} is the net cooling power of the stage, after reducing the phonon heat leak. P_{C} does not generally equal P_{NIS}, but can be a sum of several cooling power terms. Equation 15 does not explicitly depend on any phenomenological parameter, implying that the optimum O is not unique, but can be obtained with several different combinations of e.g. γ and R_{T}. It is noted that the author of this thesis is a co-author in Ref. [14], and mainly contributed to the experimental results presented.

2.1.3 Thermal model

A low-temperature refrigerator based on superconducting tunnel junctions is a multi-physics system. The cooling power in Eq. 12 is opposed by heat loads from different origins. Considering the normal metal side of a single junction, the temperature is defined separately for the electron and the phonon systems by Fermi-Dirac statistics (Eq. 1, $f(E,T)$) (electrons) and Bose-Einstein statistics (phonons). At room temperature, the two subsystems often share the same temperature due to a strong electron-phonon (e-p) coupling. The energy distribution of the electrons is influenced by electron-electron (e-e) and e-p relaxation rates which define how fast the electrons stabilize to the $f(E,T)$ after the distribution is perturbed by electron injection through the junction. At high temperature values, the e-e and the e-p relaxation rates relative to the injection rate are high. The electrons follow $f(E,T)$ and share the temperature with the phonon system. In contrast to the previous equilibrium state, a quasiequilibrium state, where the temperature of the electron and the phonon systems differ, is possible when the e-e relaxation rate remains fast but the e-p relaxation rate is slow. This case is often observed at low-temperature values. [15] Resulting temperature difference induces a heat flow between the two subsystems, which is material and geometry dependent through the coupling parameter Σ and effective volume ν. Power law model for the heat flow is given as [16]

$$P_{\text{e-ph}} = \Sigma\nu(T_{\mathrm{e}}^n - T_{\mathrm{ph}}^n). \tag{16}$$

The exponent is determined as $n = 6$ for silicon structures [17] and $n = 5$ for metal structures [18]. The coupling parameter Σ in doped silicon is a function of the doping level. Σ is measured to be 2.2 - 6.7 $\cdot$ 10^8 W/m^{-3}K^6 with doping levels of 3.5 - 16 $\cdot$ 10^{25} m^{-3} in [19]. In NIS based coolers the normal metal side's electron temperature is cooled down. In order to cool down the phonon temperature, Eq. 16 directly suggests maximizing the material dependent parameter Σ and the effective volume ν. The opposite of an equilibrium is a nonequilibrium, where the electron energy distribution does not follow $f(E,T)$ due to a slow e-e relaxation rate and high injection rate. The temperature can not be conveniently defined by $f(E,T)$ anymore.

Coupling between two phonon systems, e.g. normal metal's and thermal bath's, induces a heat flow described by a similar power law as in Eq. 16: [9]

$$P_{\text{ph-ph}} = \frac{1}{\alpha n}(T_{1,\text{ph}}^n - T_{2,\text{ph}}^n), \tag{17}$$

where α and n are material and geometry dependent parameters, and $T_{1,\text{ph}}$ ($T_{2,\text{ph}}$) is the phonon temperature of the (sub)system 1 (2). Assuming a small temperature difference $\delta T = T_{2,\text{ph}} - T_{1,\text{ph}}$, Eq. 17 can be approximated as a first order expansion in δT:

$$P_{\text{ph-ph}} = \frac{T^{n-1}}{\alpha}\delta T, \tag{18}$$

where $T = \frac{T_{1,\text{ph}}+T_{2,\text{ph}}}{2}$. Thermal resistance is then defined as

$$R_{\text{thermal}} = \frac{\delta T}{P_{\text{ph-ph}}} = \alpha T^{1-n}. \tag{19}$$

In addition to the heat flows arising from the temperature differences, Joule heating can be significant in coolers which have relatively high series resistance near the junctions. Especially in Sm-S junctions which utilize silicon as the normal metal part, the resistivity depends heavily on the doping and the final resistance is determined by the geometry. Fabrication sets limits how small the effective series resistance can be fabricated, thus it needs to be taken in to consideration especially in solutions seeking to maximize the cooling power P_{NIS} (Eq. 12) by decreasing the tunneling resistance R_{T}. Joule heating in the series resistance R_{series} with current I is given by Joule's law:

$$P_{\text{Joule}} = R_{\text{series}} I^2. \tag{20}$$

Thermal model of a NIS refrigerator is shown in Fig. 6. Heat is extracted from the normal metal's electron system to the superconductor's electron system by P_{NIS}. Electron-electron (e-e) relaxation is assumed to be fast enough for the temperature $T_{\text{N,e}}$ to be defined. The refrigerator is thermally connected to the thermal bath, usually cryostat flange. Thermal bath is assumed to have strong enough electron-phonon for equilibrium state, thus sharing equal electron and phonon temperature. The superconductor is often thermalized to the bath so that the phonon heat flow is between the bath, the superconductor and the normal metal, characterized by $P_{\text{ph-ph}}$. Thermal resistance is generally negligible between the bath and the superconductor, leaving the main thermal resistance between the superconductor and the normal metal. Especially in this thesis, this thermal resistance can be assumed to lie mostly on the interface between the superconductor and the normal metal. Interfacial thermal resistance or Kapitza resistance is given as:

$$R_{\text{Kapitza}} = R_{\text{thermal}} A, \tag{21}$$

where A is the interface area. An acoustic propagation mismatch between the two materials on other sides of the interface gives rise to the Kapitza resistance.[3]

Other mechanisms which induce effective heat flows, are quasiparticle backflow and recombination, coupling to the electromagnetic environment and Andreev reflection.

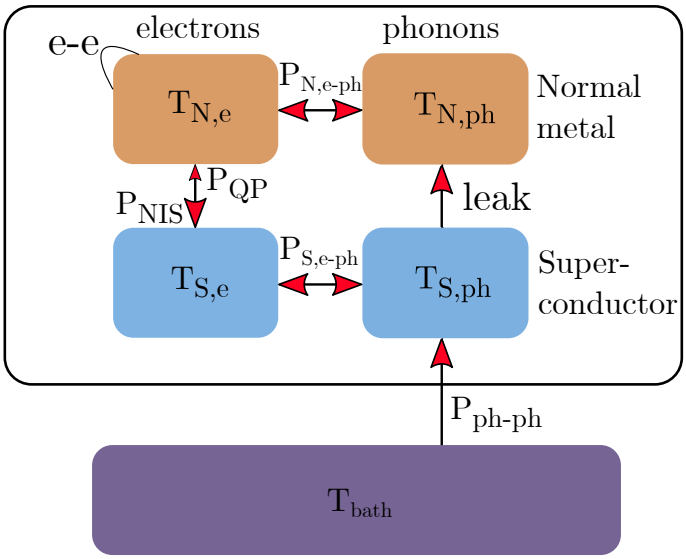

Figure 6: Thermal model of a NIS refrigerator. Electron and phonon systems in normal metal (N) and superconductor (S) are in quasiequilibrium, coupled by different heat flows.

Hot quasiparticles (electron-like) in the superconductor can tunnel back to the normal metal, generating backflow heat current [16]. The heat flow accompanied by the quasiparticle backflow can be given by: [20]

$$P_{\mathrm{QP}} = \beta(IV + P_{\mathrm{NIS}}), \tag{22}$$

where the phenomenological parameter β is around 0.01 - 0.05 for aluminum systems. Equation 22 does not provide insight to the physical phenomena of back-tunneling, but gives a way to model the measured data more accurately. In quasiparticle recombination, two quasiparticles in the superconductor form a Cooper pair emitting a phonon with an energy of 2Δ. Electromagnetic environment can trigger photon assisted tunneling in the junction, forcing low energy electron tunneling across the junction. [3, 21]. Andreev reflection is a two-particle transport process, unlike all before mentioned mechanisms, where a Cooper pair is destroyed (formed) and by the current conservation two single particles are formed (destroyed) on the normal metal. Current induced by the Andreev reflection is generally dominated by the single particle transport, but with highly transparent junctions (small R_{T}) and with near zero bias voltages, the Andreev current can be observed as a reduced resistance at low temperature values. The Andreev current induces a heat current which leads to dissipation in the normal metal. [18, 22, 23, 24] In the thermal model this heat current is neglected.

In addition to the strong e-ph coupling in the normal metal, an ideal NIS cooler should minimize the heat leak between the phonon systems of the superconductor and the normal metal. In this thesis, the leak is studied and aimed to be decreased. So-called quasiparticle traps can be tailored to diffuse the energetic quasiparticles away from the junction [25, 26], reducing the back-tunneling current and the associated heat

flow. The traps are made from normal metal and placed next to the superconductor. Importantly, the traps are essential for the hot quasiparticle thermalization as the e-ph coupling in superconductors is exponentially suppressed at low-temperature values.

2.2 Flip-chip technology

Chip-level interconnection techniques can be divided to three main categories: wirebonding, tape-automated bonding and flip-chip bonding. Schematic in Fig. 7 shows the basic idea of each method. In wirebonding, the chip is connected to the substrate or readout-chip by an electrically conducting wire, often made from gold, aluminum or copper. The method is vastly used from 1950s to the present day in the microelectronics industry due to its flexibility and low defect ratio. Disadvantages include large footprint area required for the bonding pads, slow process rate due to each wire end being bonded separately and poor electrical performance from long and thin wires. Delicate wires are also susceptible to mechanical failures due to vibrations and brittle alloys. To tackle these problems, tape-automated bonding (TAB) was developed by General Electric in the 1960s. TAB utilizes a flexible Printed Circuit Board (PCB) with small conductive dies, which are bonded to the chip and the substrate all at the same time. The method allows better electrical- and thermal performance, improved mechanical stability and faster bonding compared to the wirebonding. Adding the third circuit in addition to the chip and the substrate however increases the complexity and processing steps significantly. [27]

In 1964, IBM introduced it's newly developed bonding process, flip-chip bonding or Controlled Collapse Chip Connection (C4) [28]. The flip-chip technology reduces the complexity of the chip-level packaging by bonding the chip directly on the substrate. The name, flip-chip, comes from the idea of flipping the chip and bonding it upside down to the substrate. The technology provides lower cost by getting rid of external wires and circuits, increased electrical- and thermal performance due to minimized path length from the chip to the substrate and good mechanical resistance. The flip-chip bonding allows easier 3D assembly of integrated circuits, as the chips can be stacked vertically on top of each other. [27] In this thesis, flip-chip technique is used and studied for the vertical integration of superconducting solid state microcoolers. The ultimate advantage of using a flip-chip bonding in case of coolers is the possibility to place an additional chip or device on top of the cooler.

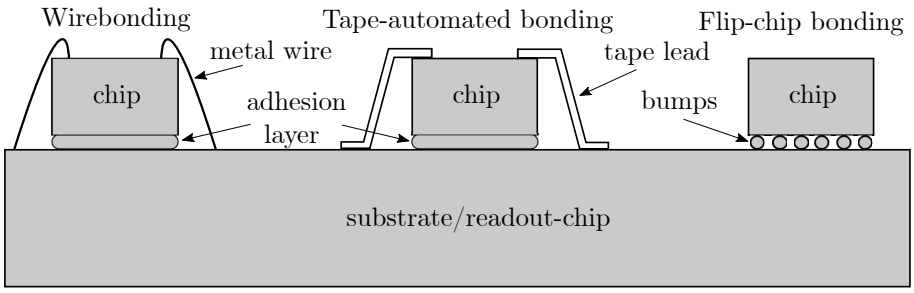

Figure 7: Three main chip-level interconnection techniques visualised. Both in wirebonding and tape-automated bonding the chip is attached to the substrate with external adhesion layer, such as glue. In flip-chip bonding the adhesion is established with the bumps responsible for electrical and thermal connection.

2.2.1 Flip-chip bonding

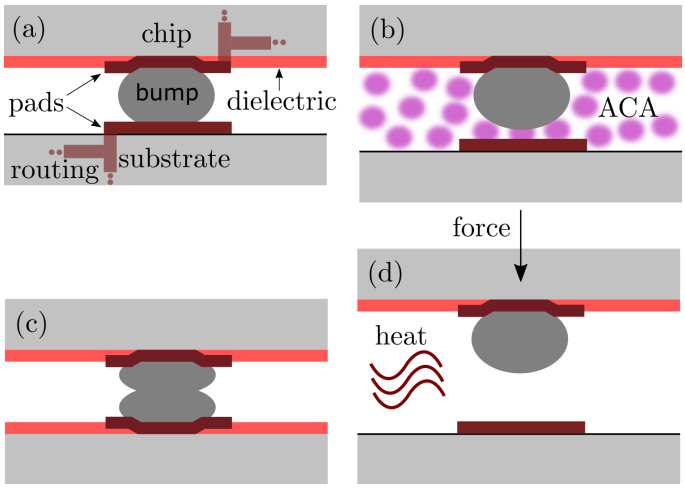

Figure 8: Cross-section schematics of different flip-chip bonded packages (a-c) and illustration of thermocompression bonding process (d). Structures are highly simplified for clarity. (a): Bond formed between the chip and the substrate by bump deposited on the chip side. Pads are conductive layers connected to other pads by routing suitable for the application. Dielectric layer separates pads from each other galvanically. (b): Bond formed by Anisotropically Conductive Adhesive (ACA) placed between the chip and the substrate. (c): Bond formed by bumps on both sides. (d): Thermocompression bonding, where static force is applied in addition to heat to bond the bump to the opposite pad.

Figure 8 illustrates a few different cross-section schematics (a-c) and thermocompression bonding (d) in a single bond level. In Fig. 8(a), the bump has been deposited on a conductive pad on the chip. A dielectric layer is cutting the galvanic contact between separate pads and inhibiting diffusion processes between the chip/substrate material and other layers. The bump is in direct contact with the pad on the substrate, forming a good electrical and thermal contact. Note that often a separate Under Bump Metallization (UBM) layer is used between the bump and the pad to provide better adhesion. Different layers are discussed more in the next section. Routing from pad to pad on the chip can be done in various methods, using Through Silicon Vias (TSVs), lithography methods or with standard PCBs, for example. The same applies for the substrate. The contact between the bump and the substrate pad is made by using a reflow technique, analogous to a common soldering. First, the chip and the substrate are aligned properly, and then pressed on to each other. At this point, temperature is often raised near the melting point of the bump material. Afterwards, the bonded package is placed in oven filled with inert gas and heated over the melting point of bump material in order to form a final reflow bond. The cavity between the chip and the substrate can be filled with an underfill glue to enhance mechanical stability by reducing stress on the bumps. [27]

In Fig. 8(b), the contact between the bump and the substrate pad is achieved using an anisotropically conductive adhesive (ACA). ACA is a special kind of glue,

which only conducts electricity in a vertical axis, preventing lateral electrical shorts between separate pads. Using the ACA method has several advantages over the standard reflow method. The reflow method requires using high temperature, near the melting point of the bump. The melting point is material dependent, and for usual soldering materials it ranges from 240 °C of pure tin (Sn) to 400 °C of gold-tin alloy. High temperature can critically damage others parts of the substrate-chip -structure, making it unusable. The ACA method requires processing temperature of less than 150 °C, making it feasible for delicate structures. The reflow method additionally requires use of soldering flux, which prevents oxidization of metals at high temperature and improves wetting properties of the bump. Wetting of bumps determines the contact made between the bump and the pad in reflow. The ACA method eliminates the use of flux and the underfill, as the adhesive glue acts as a mechanical support as well. [27]

In addition to the previously described methods with bumps deposited on the chip side, Fig. 8(c) shows a bump-to-bump bonding method. Both the chip and the substrate have bumps deposited and the bond is formed between the bumps. Both the reflow and the ACA methods can be used with bump-to-bump bonding.

Figure 8(d) shows a simple schematic for single bump thermocompression. In thermocompression, the chip is, additionally to the heating, pressed by a static force for given time on to the substrate to form a bond. Thermocompression efficiently decreases the process temperature needed by deforming the bumps with external pressure. The method is specifically useful with ductile and soft bump materials, such as indium. Indium's melting point is near 155 °C, but it has a remarkable property of cold welding to itself. [29] Direct heating in thermocompression can also be replaced or accompanied by ultrasonic vibrations, if the materials can not withstand high temperature [30].

In this thesis, the flip-chip bonding method is bump-to-bump bonding by thermocompression just above the room temperature in atmospheric environment. The specific method is described fully in Sect. 3.1.3.

3 Experimental methods

3.1 Fabrication

A single vertical cooler consists of two parts: A substrate and a top-chip. The two are interconnected in a flip-chip bonding process. The substrate is the one providing a routing between the junctions, electrical connection pads for the measurement setup and a thermalization channel to the thermal bath. The top-chip contains the superconducting tunnel junctions, where the normal metal side is doped silicon and the superconductor in this thesis is aluminum.

A single device contains a series of tunnel junctions. The series connection is achieved by interconnecting the substrate and the top-chip with the indium bumps, and isolating the adjacent bumps and pads from creating electrical shorts. The fabrication process of the substrate and the top-chip, and interconnecting them is discussed next.

3.1.1 Substrate

The fabrication process of the substrate is depicted in Fig. 9 in seven main parts. (1) The process starts with a standard 675 µm thick P-type silicon wafer. The wafer is cleaned and the native oxide is etched away. (2) 100 nm of dry thermal oxide is grown epitaxially to isolate the rest of the stack from the silicon. (3) Next, 200 nm of Al and 25 nm of Ti are deposited on top by sputtering. Ti functions as an adhesion layer for the indium bumps, and Al increases electrical conductivity. (4) Pads are formed and galvanically isolated with metal etching all the way to the oxide layer. (5) Lift-off resist is deposited on top, the indium bump positions are patterned with lithographic methods and developed. (6) Indium layer with a target thickness of 3.5 µm is evaporated on top and (7) finally lift-off is performed by immersing the full wafer in acetone while applying ultrasound.

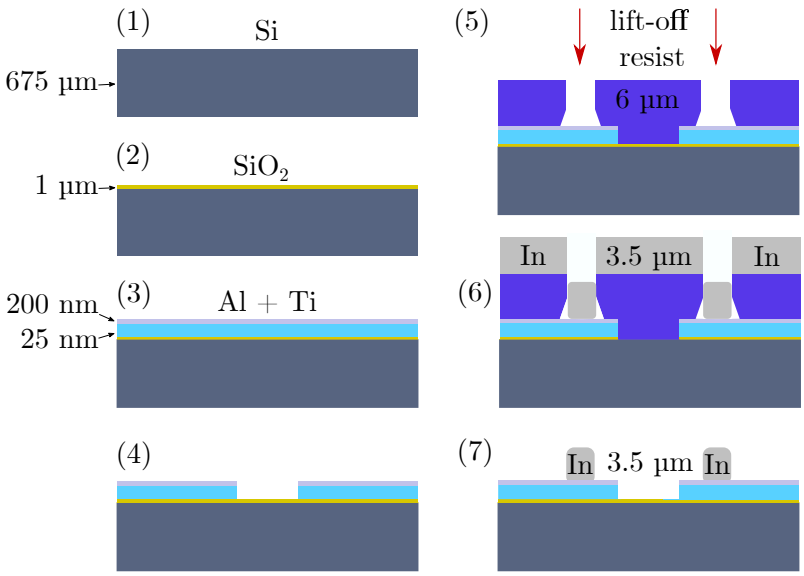

Figure 9: Process of flow of the substrate. Single cell is shown, but the process is wafer scale. (1): P-type silicon wafer with a thickness of 675 µm. (2): 1 µm of dry thermal oxide is grown on top. (3): Superconductor (200 nm of Al) and adhesion layer (25 nm of Ti) are deposited on top. (4): Lithographic patterning and metal etching to separate the pads. (5): 6 µm of lift-off resist is spun, exposed and developed to pattern indium bump positions. (6): Indium deposition by evaporation with a target thickness of 3.5 µm. (7): Lift-off and the final product.

3.1.2 Top-chip

Summary of the top-chip's process flow is depicted in Fig. 10. The top-chip, containing the tunnel junctions, is fabricated on a red phosphorous doped Silicon-on-Insulator (SOI) wafer. The SOI wafer (1) has a protective oxide coating on the back, a handle of 500 µm with a resistivity of smaller than 1.5 mΩcm, an insulating layer of Silicon Oxide (SiO_2) of 1 µm and a top layer of 40 µm with a resistivity smaller than 1.5 mΩcm. (2) Superconductor and bump adhesion layers are deposited next by sputtering. In this thesis, the sample has 500 nm Al layer as superconductor and 25 nm layer of Ti as the adhesion layer. (3) Metal layers are plasma etched and (4) deep reactive ion etching (DRIE) is used to galvanically isolate the islands from each other. DRIE etching needs to reach the SiO_2 layer to be successful. Finally, lift-off resist is spun to the wafer and lithographically patterned. (5) Indium is evaporated on top with target value of 3.5 µm and lift-off is performed to complete the process.

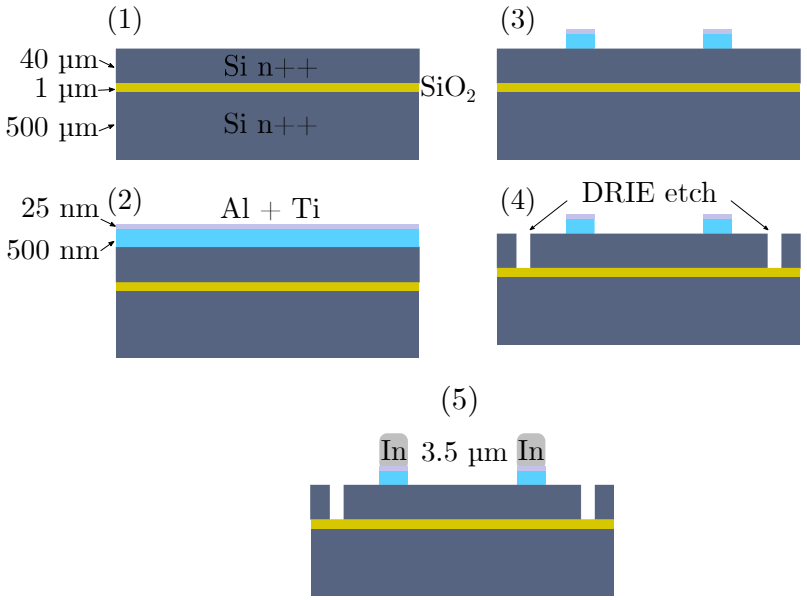

Figure 10: Process flow of the single cell of top-chip. (1): Flow starts with the standard SOI wafer. (2): Superconductor (500 nm Al) and bump adhesion layer (25 nm Ti) are deposited on top. (3): Metals are patterned with plasma etching. (4): DRIE etching is used to galvanically isolate islands from each other. (5): Indium bumps are built by evaporation, patterning and lift-off.

3.1.3 Bonding

Integration of the substrate and the top-chip is done with a semiautomatic flip-chip bonder FC150 from SET. First, the specific vacuum tools and a chip tray are chosen. The vacuum tools are made from Silicon Carbide (SiC), which has a high thermal conductance, but a low thermal expansion coefficient. Vacuum tools are used to keep the substrate and the top-chip on place, and the thermal properties allow heating the chips through the tools efficiently, without biasing the chip alignment. The chip tray is used to place the top-chip on a well-defined position for the bonding arm to pick the chip up. The bonding arm is responsible for controlling the bonding force and moving the top-chip along the z-axis. Once the tools are in place, the substrate is put on top of the vacuum tool on a substrate chuck facing up. Now the bonding cycle can be started.

Before the actual bonding, the substrate and the top-chip have to be aligned in the x-y -plane and levelled. The set-up is shown in Fig. 11. Vacuum tools are used to hold the substrate and the top-chip in place and a microscope is slid between the two. The substrate and the top-chip are aligned manually by first matching the bumps on the bottom left corner, then moving the microscope to the top right corner and matching the bumps again. With this input, the FC150's alignment algorithm rotates the substrate to match the made corrections. The procedure is iterated several times to make the alignment more precise. The levelling is done with an autocollimator, which illuminates a light beam on the back of the substrate/top-chip and records the reflection. The reflected beams are shown on the computer screen and manually adjusted on top each-other, which levels the substrate and the top-chip parallel to each other. Failure in levelling results in uneven distribution of force when bonding. Uneven force compresses bumps on one side of the chips more than on the other side, which can result in electrical shorts when the bumps expand too much laterally and touch each other.

After careful and precise alignment and levelling, the bonding can proceed. The bonding arm lowers the top-chip towards the substrate slowly, and when it senses a force equivalent to 10 grams, the substrate and the top-chip are heated to the set temperature for a given time interval. The force starts to ramp up linearly towards the defined value, always overshooting 1-2 %. The force is kept steady for the set time, and then released. The temperature is lowered back to room temperature and the vacuum holds are released, completing the bonding. Example of a thermocompression cycle used in this work is given in Fig. 12. The cycle ends when the bonding arm has returned the top-chip vacuum tool back to its tool rack and the chuck has returned to the starting position. The flip-chip assembly can be removed with tweezers, and the next pair of substrate and top-chip can be immediately loaded to the bonder.

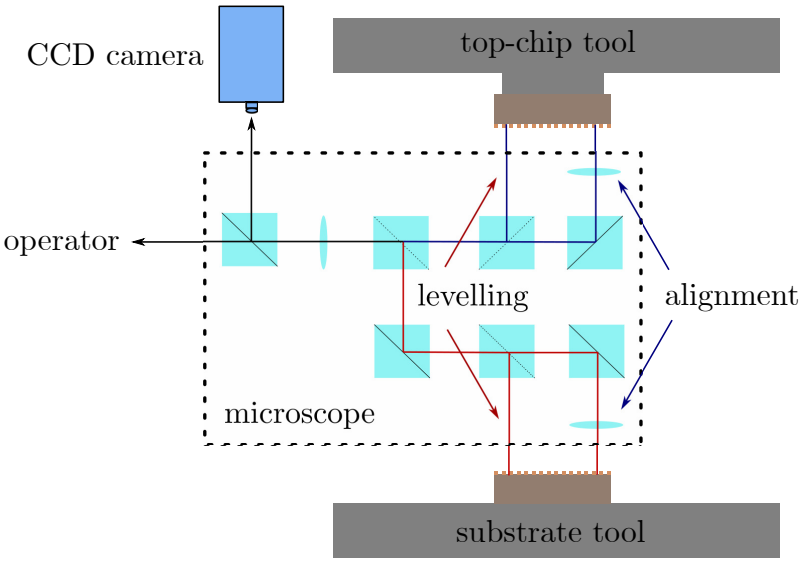

Figure 11: Alignment and levelling set-up of the flip-bonder FC150. The microscope is placed between the substrate and the top-chip. A CCD camera and direct view for the operator are used to manually align and level the chips.

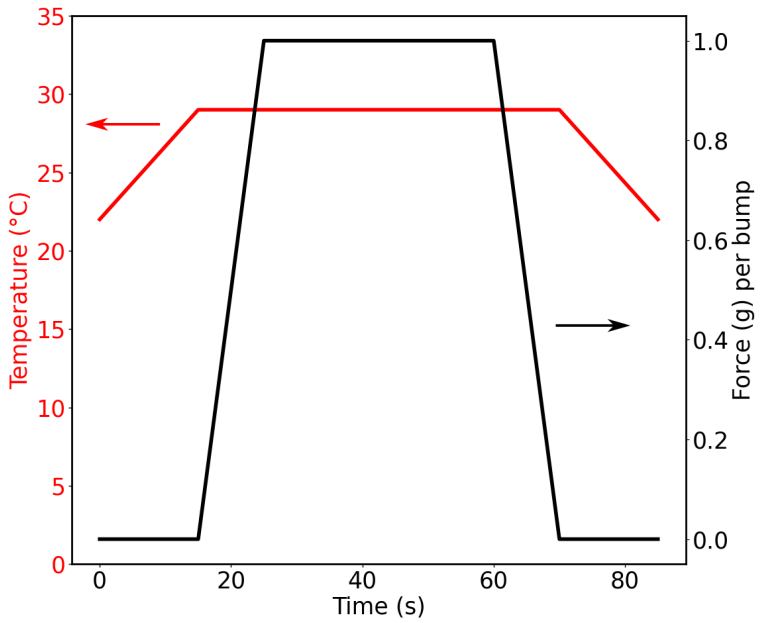

Figure 12: Typical thermocompression cycle with temperature (red) and force (black) as a function of time. Temperature is elevated from room temperature to 29 °C and the force is increased to 1 g per bump. Both parameters are kept constant for a set period of time and then relaxed to the starting values.

3.2 Cryogenics

Cryogenic methods are needed to reach the thermal operation range of the devices characterized in the thesis. The temperature range is defined by experiment, but the highest typical value is at the critical temperature of superconductor and the lower limit to the base temperature of the cryostat. As the superconducting gap evolves as a function of the temperature below the critical temperature, stable temperature control is also needed to study different operation points of the device.

Since the liquification of helium in 1908 and discovery of superconductivity in 1911 by K. Onnes [31], refrigeration methods have developed rapidly. Dilution refrigerators have become a standard in experimental low-temperature physics. They produce continuous cooling at base temperature of milliKelvin range. Alternative to the dilution refrigerators are helium-3 refrigerators. They provide cooling by liquifying the helium-3 and pumping the bath, creating evaporative cooling and reaching a base temperature of around 300 mK. These single-shot refrigerators provide cooling until all of the liquid helium-3 is evaporated.

In this thesis, the dilution refrigerator is model LD250 from Bluefors. LD250 provides 250 µW of cooling power at 100 mK and is able to reach a base temperature of 10 mK. The second refrigerator used is a ^{3}He adsorption cryostat from Oxford Instruments, model Heliox AC-V. Both of the refrigerators are closed cycle coolers or cryogen-free refrigerators, meaning that they don't require filling with liquid helium. A separate pulse tube cooler is used for pre-cooling to achieve liquid helium temperature in both refrigerator types. A standard pulse tube cooler is a closed-loop helium cooler, where the helium is compressed and the resulting heat is removed via a heat exchanger. The compressed helium is fed to the cold head or pulse tube head and expanded there, providing cooling by adiabatic expansion. The expanded helium is fed back to the compressor through a rotary valve and the circulation starts again. The rotary valve is responsible for cyclic pressure wave, which pumps heat away from the cooled object.

3.2.1 Heliox AC-V

A base temperature of 300 mK and highly automated temperature control up to tens of Kelvins of the ^{3}He adsorption cryostat provides excellent conditions for characterizing tunnel junctions and coolers based on them. The Heliox AC-V is pictured in Fig. 13, excluding radiation/vacuum shields and experimental wiring. The temperature is reduced gradually in the cryostat. The room temperature plate or the 300 K plate is located upmost, where the line inputs for experimental wiring and temperature control are located. The pulse tube cold head is placed on top of the 300 K plate and the helium is pumped through the thinner pulse tube pipes and returned through the wider pipes. Previously explained pulse tube cooling cools the first pulse tube stage temperature down to 50 K and the second stage down to 2.6 K. The second stage is able to liquify or condense the helium-3 to the ^{3}He pot, where the samples are mounted. The critical temperature for the helium-3 is 3.35 K and it is liquified at 3.2 K. The helium-3 is contained in a closed system starting from a ^{3}He dump, which is thermalized to the 50 K plate. The dump is connected to an adsorption pump through an over-pressure safety valve, a manual dump valve and a manometer. A heat switch is used to cool down the adsorption pump to below 10 K, enabling pumping of the liquid ^{3}He bath. The heat switch contains ^{4}He which is heated to gas for providing a thermal link inside the switch. In contrast, when the switch is not heated and let to cool down via the 2.6 K plate, the ^{4}He is liquified to cut the thermal link. Adsorption pump and the ^{3}He pot can also be heated to control the temperature.

The cooldown starts by pumping high vacuum inside the refrigerator with an external back-end pump and turbo pump. The pulse tube is started and the system is let to cool down overnight. Final pressure should be around 10^{-6} to 10^{-7} mbar and the pulse tube temperature near 2.6 K. Cooling down the system provides additional decrease in the pressure, as the gases present are condensed on the cold surfaces, which is also called cryopumping. The mechanical vacuum pumps are removed and the ^{3}He dump valve opened. Helium-3 will expand from the dump to the system, and start cooling down. The ^{3}He precooling takes around two days due to the heat needed to sink from the ^{3}He pot, which is essentially half a kilogram of copper. The final temperature of the ^{3}He pot should be below 5 K, depending on the performance of the pulse tube. The ^{3}He valve is closed and the adsorption pump is heated up in order to emit all the helium-3 gas to the system. The 2.6 K plate will now condense the helium-3. For the final step, the adsorption pump is cooled down through the heat switch to less than 10 K. Cold adsorption pump pumps the liquid-vapour interface in the ^{3}He pot, resulting in evaporative cooling with power $\dot{Q}_{\text{evap}}$ proportional to the latent heat L and the vapour pressure P_{vap} of helium-3:

$$\dot{Q}_{\text{evap}} \propto LP_{\text{vap}} \propto e^{-1/T}. \tag{23}$$

The cooling power reduces exponentially as a function of the temperature of the liquid, as the vapour pressure decreases. The latent heat of evaporation and the vapour pressure are related by the Clausius–Clapeyron equation. Ultimately the evaporative cooling power equals the heat leaks to the liquid helium-3, and the

temperature can not be decreased further. The liquid helium-3 efficiently determines the temperature of the copper ^{3}He pot and the samples attached to it, as the specific heat capacity of the liquid helium-3 (≈ 1 J/(g·K)) is orders of magnitude higher than the corresponding value for copper ($\approx 10^{-5}$ J/(g·K))) at Kelvin temperatures. [8]

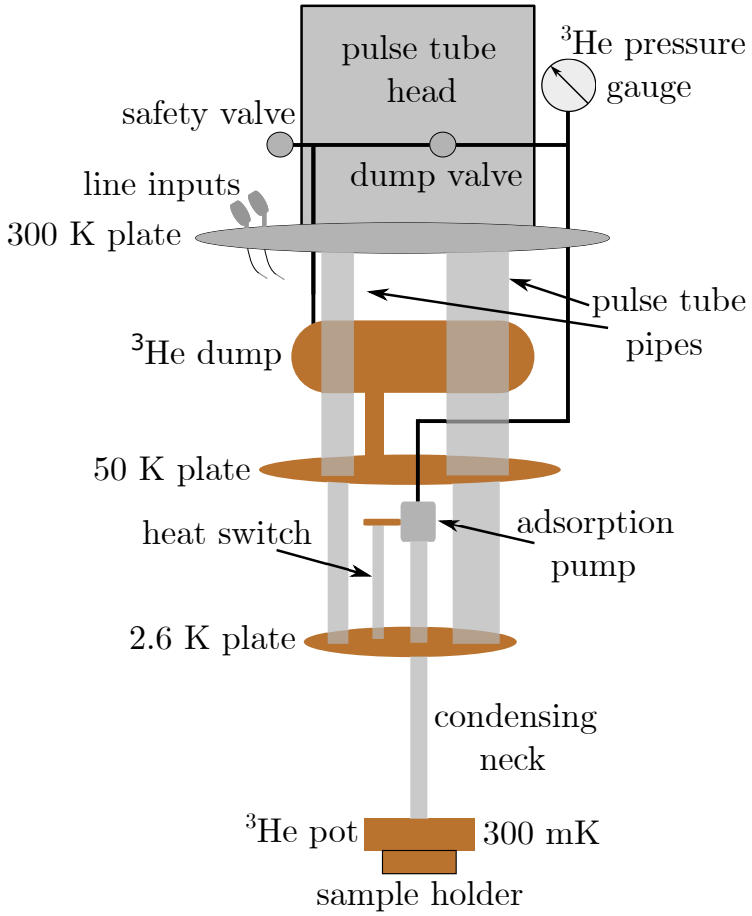

Figure 13: Schematic of Heliox AC-V without vacuum/radiation shields attached. The temperature is reduced gradually from 300 K to 50 K and 2.6 K by a pulse tube cooler. The base temperature of 300 mK is reached in the ^{3}He pot where the liquid ^{3}He is cooled by forced evaporation.

3.2.2 LD250

Continuous low-temperature part cooling cycle of a dilution refrigerator is depicted in Fig. 14. Similarly with Heliox AC-V discussed in the previous section, LD250 uses a pulse-tube cooler to reach the temperature of liquid helium. From there, the dilution cycle starts and cools down typically to 8-10 mK. The samples are mounted on the 10 mK plate. Experimental wiring, heater, and thermometry wiring are fed through several flanges at different temperature values. The wires are thermalized at every intermediate temperature and the feedthroughs are radiation isolated to minimize heat leaks. The LD250 is a closed-cycle refrigerator, but still requires external filling of so-called cold trap with liquid nitrogen. Cold trap's function is to clear contaminants by freezing them from the ^{3}He/^{4}He mixture circulating in the dilution part. [32]

Once the mixture is pre-cooled by the pulse tube to a temperature lower than 4.2 K, the mixture is compressed to a pressure of 2 bar and then cooled further down by driving it through a main flow impedance and heat exchanger. The mixture is flowed through a nozzle and expanded, resulting in cooling by the Joule-Thomson effect. The mixture is condensed, filling the still, mixing chamber and the lines in between. Now the dilution cycle is started by pumping the still with turbo and scroll pumps. Evaporative cooling cools down the liquid mixture in the still further to 700 mK and the heavier isotope helium-4 is collected on the bottom of the mixing chamber. Two phases are formed in the system, the dilute phase and the concentrated phase. The dilute phase is richer in helium-4 and the concentrated phase in helium-3. Pumping the separated phases in the still results in helium-3 extraction, diluting the mixture even further. The pumped helium-3 is purified in the cold trap and injected back to the system, thermalized through the still and heat exchanger between the incoming and outcoming flows. The heat flows are indicated by the red arrows and the direction of the mixture flow is depicted by the blue arrows. Once the concentrated phase enters the mixing chamber, the helium-3 atoms are forced to mix to the diluted phase. Due to the higher enthalpy in the diluted phase compared to the concentrated phase, cooling will occur. Naturally the cooling power depends directly on the helium-3 flow rate through the phase boundary. The flow rate can be enhanced by increasing the evaporation rate in the still. Still can be heated to increase the vapour pressure, resulting in increased evaporation. The circulation is completed by pumping the helium-3 from the diluted phase back to the still, driven by the osmotic pressure generated in the still due to the helium-3 evaporation. [32] The cooling power of the dilution process is given by [8]

$$\dot{Q}_{\text{dilut}} = \dot{n}_3[H_{3,\text{d}}(T) - H_3(T)] \propto T^2, \tag{24}$$

where $\dot{n}_3$ is the helium-3 rate from the concentrated phase to the diluted phase in moles per unit time, $H_{3,\text{d}}(T)$ is the temperature dependent enthalpy of helium-3 in the diluted phase and $H_3(T)$ is the temperature dependent enthalpy of the helium-3 in the concentrated phase. The T^2 proportionality comes from the helium-3 enthalpy dependencies. A practical limit for the dilution cooling power is set by the efficiency of heat exchangers and the pumping rate of the still.

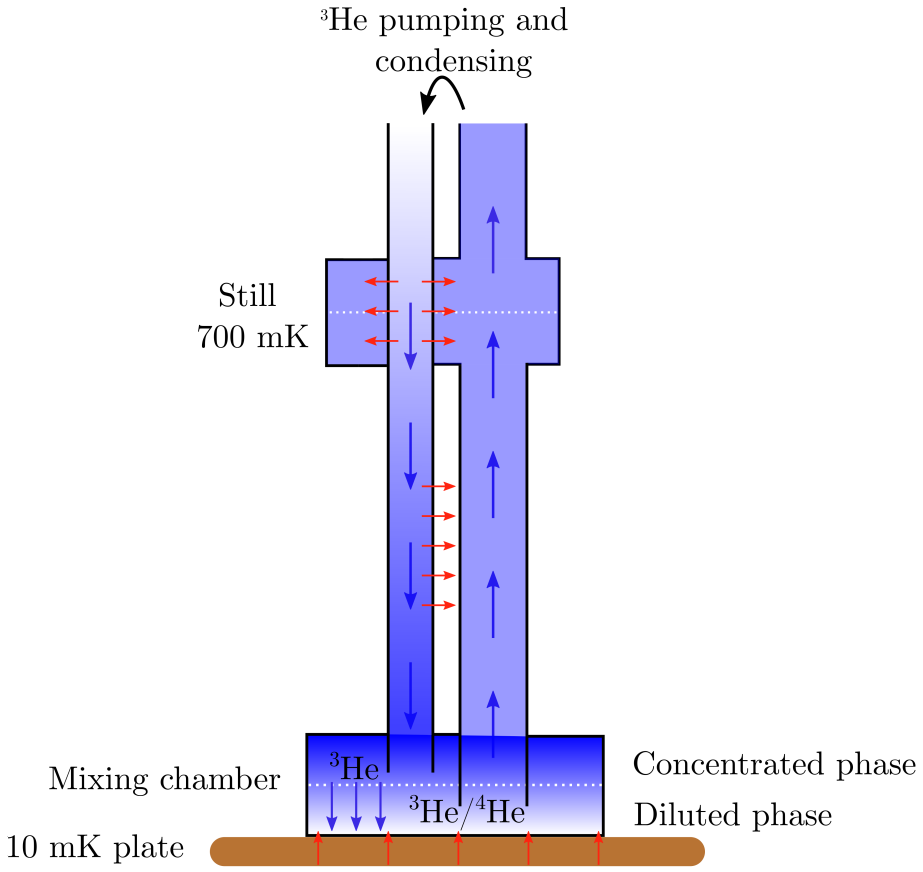

Figure 14: Closed dilution cycle of ^{3}He/^{4}He mixture. Blue arrows indicate the flow of helium-3 and red arrows indicate heat flow. Dotted white line in still and mixing chamber is the phase boundary of the concentrated and diluted phases. 10 mK plate is cooled by the dilution process in the mixing chamber. Osmotic pressure drives the helium-3 from the diluted phase back to the still and it is evaporated, and condensed back to the circulation.

3.3 Measurements

Low-level electrical measurements as a function of temperature are conducted by placing the device under test in the cryostat. The measurement equipment is controlled through a LAN connection, allowing tracking and logging the data remotely outside the lab. Custom scripts supported by Python library *QCoDeS* [33] are used to perform automated measurement sweeps in current, voltage and temperature.

3.3.1 Electrical characterization

Standard current-voltage (IV) characteristics are measured to rate the quality of the samples. Tunnel junction parameters R_T, γ and Δ are obtained by measuring voltage over the sample as a function of a current bias. Measurement scheme for current biasing the sample is depicted in Fig. 15. A programmable voltage source is used to supply DC voltage, which is converted to a current via the bias resistor. Bias resistor's resistance is orders of magnitude larger compared to the resistance in rest of the current path. The sample is mounted inside the cryostat to the bath temperature. The sample consist of one or several junctions in series. The current I is converted and amplified to the voltage $V_2(I)$ with a transimpedance amplifier, and the resulting current dependent voltage is measured with a digital multimeter (DMM). Gain of the transimpedance amplifier determines the current from the measured voltage. The gain is proportional to the transimpedance resistance R_f Increasing the amount of junctions in the chain increases the total resistance, and the current bias might not be well defined anymore when the sample resistance approaches the bias resistance. With high resistance samples, it is desirable to remove the bias resistor and bias the sample with voltage. The voltage over the sample is measured with a separate voltage amplifier and DMM to obtain the four-wire resistance of the sample.

Current biasing allows approximating the current without measuring it. Assuming bias resistance to be orders of magnitude higher than the resistance in the rest of the circuit gives the current directly with Ohm's law $I_{\text{bias}} = U/R_{\text{bias}}$, where U is the voltage supplied. Removing the transimpedance amplifier and the DMM ($V_2(I)$) can effectively reduce noise e.g. through removing ground loops and pick-up noise. Similarly, assuming the sample's resistance to be orders of magnitude higher compared to the rest of the circuit, voltage over the sample can be approximated to be directly U, which removes the need for measuring V separately.

In addition to the DC biasing, adding a small AC current excitation with a fixed frequency allows probing the differential conductance as a function of the DC bias. Resulting AC voltage over the sample can be sampled with a standard DMM and the fixed frequency component is isolated utilizing a Fourier transform. In this thesis, the AC voltage is measured with a lock-in amplifier using homodyne detection. The amplifier is able to extract the frequency component which was supplied to the circuit and ignore the rest, reducing the noise carried by other frequencies from the signal. However, the noise present in the circuit affects the sample and, for example, can alter the operation point of the device under test or generate heating.

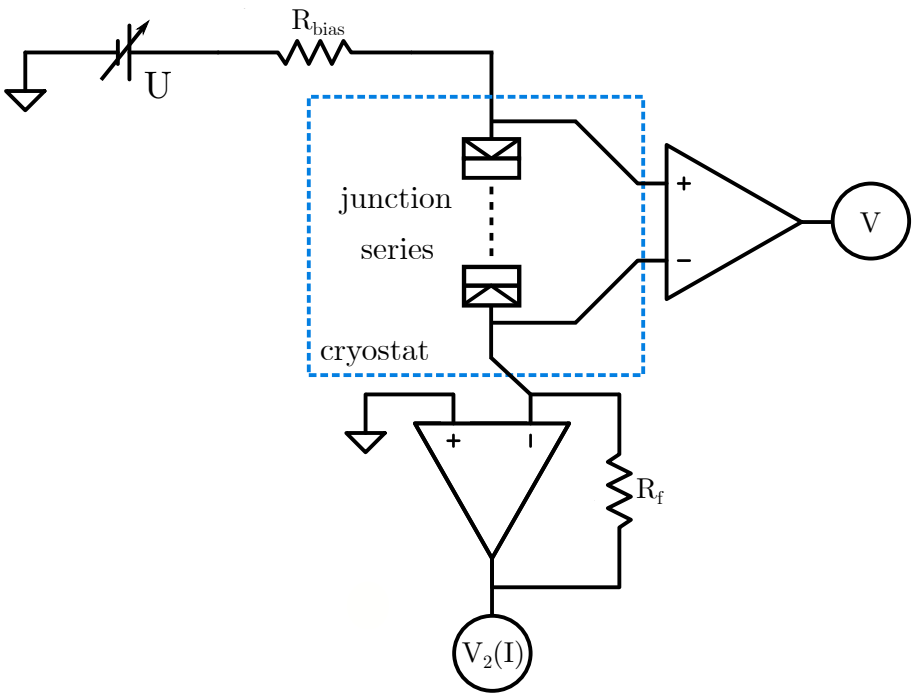

Figure 15: Four-wire IV measurement circuit using current bias. Voltage U is converted to a current through a large bias resistor R_{bias} and in to the cryostat through the sample consisting of junctions in series. The current is recorded by converting it to a voltage with a transimpedance amplifier. The converted voltage is measured with a digital multimeter, giving the current information together with the amplifier's gain. The voltage is measured with a floating configuration across the sample.

3.3.2 Thermal performance

As discussed in Sect. 2.1.3, the interplay of different heat flows determines the performance of a microcooler based on superconducting tunnel junctions. Thermal performance of vertically integrated samples is studied by determining the thermal resistance or measuring the cooling performance.

Thermal resistance is measured by biasing a chain of junctions outside the sub-gap regime i.e. with $|V| > \Delta_0/e$ and recording the resulting electron temperature with another junction pair. Cooling instead is observed near the gap edge. The set-up is divided in two parts: the heater and the thermometer, as shown in Fig. 16. In this thesis, only the thermal resistance is determined.

The heater is symmetrically DC current biased with a floating voltage supply configuration and voltage over the sample is measured as discussed in the previous section. The thermometer is current biased with a fixed AC current as described in Sect. 2.1.1. The resulting voltage response dV is recorded with an AC coupled lock-in amplifier. The thermometer could also be DC biased, but using AC allows decoupling the DC signals from the measurement of the temperature. The configuration here relies on the assumption that the heater/cooler and the thermometer are galvanically

isolated, and the heat is transferred from one to another efficiently via phonons in the top-chip, isolated from substrate phonons.

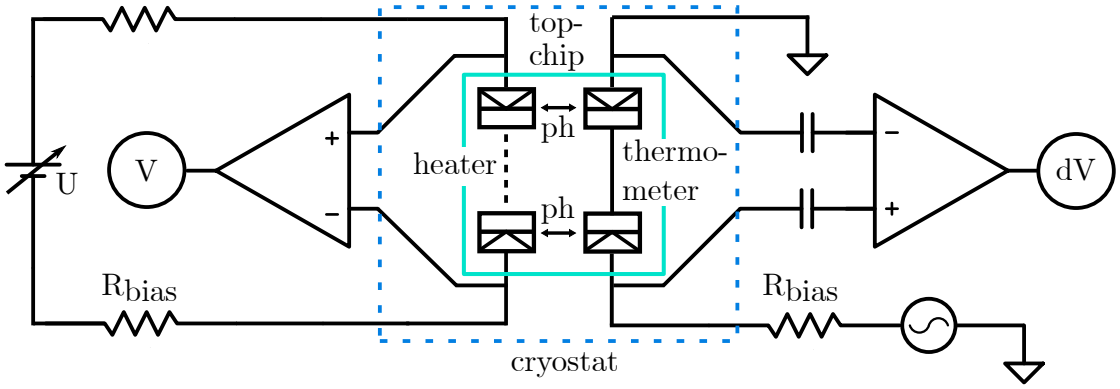

Figure 16: Measurement scheme where the series of junctions is used as a heater or a cooler and the resulting temperature is recorded with another pair of junctions. Heater/cooler is symmetrically DC current biased and the thermometer is AC current biased.

4 Results

Quality assurance for the flip-chip samples following the fabrication process presented in Sect. 3.1 is presented before the analysis of the thermal resistance. The single islands on the top-chip are not galvanically isolated due to flawed DRIE etching, leading to the problem that the whole junction chain could not be used. One pair of junctions is used as a heater and another pair is used as a thermometer in the thermal resistance measurements.

4.1 Quality assurance

4.1.1 Prior bonding

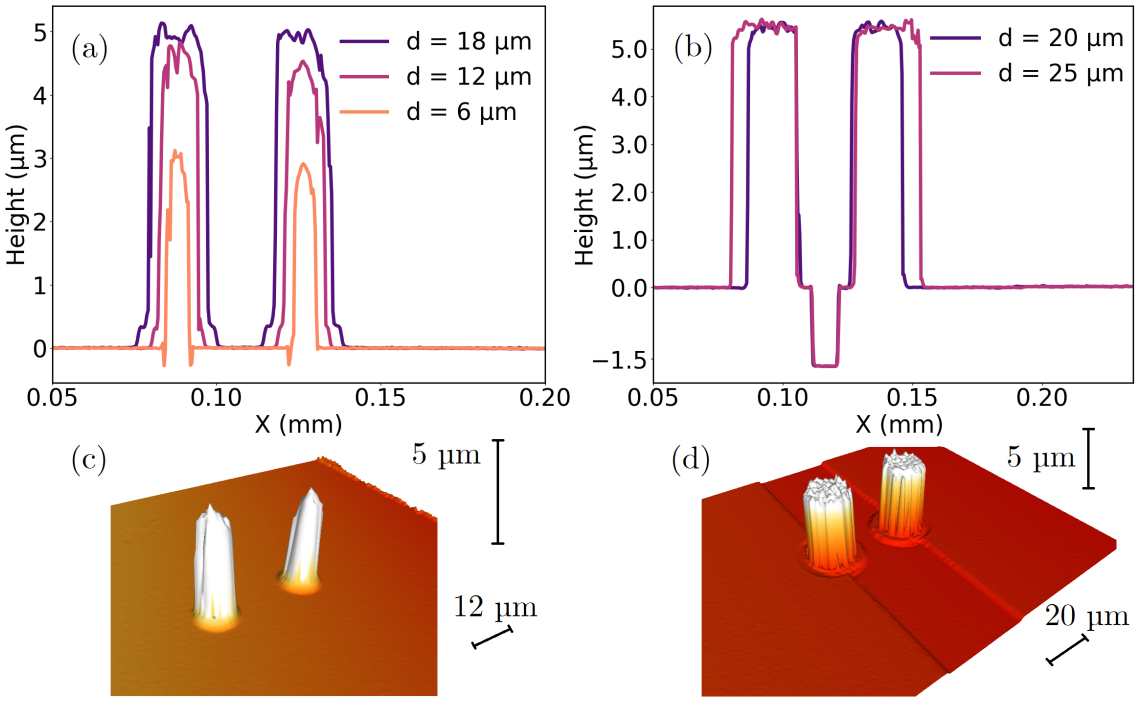

Figure 17: Pre-bonding height profiles for bumps with diameters of (a): 6, 12 and 18 µm and (b): 20 µm and 25 µm. 3D profiles by optical profilometer with bump diameters of (c): 12 µm and (d): 20 µm.

Before bonding, five different bump sizes are investigated. Height profiles measured with an optical profilometer of the top-chip bumps with diameters of 6 µm, 12 µm and 18 µm, and substrate bumps with diameters of 20 µm and 25 µm are shown in Fig. 17. (a) and (b) show the height profiles. (c) and (d) illustrate the 3D profiles. The target bump height in the evaporation process is 3.5 µm, but deviation from the target is observed. The height is seen to be a function of the bump width, where 6 µm bumps are below the target, while 12 µm and 18 µm are above the target height. Instead, 20 µm and 25 µm bumps are equal in height, around 5.3 µm. Additionally, the apical curvature of the bump is seen to be higher in bumps with smaller diameter.

Both observations can be explained by the evaporation process. Evaporated indium does not enter the opening in lift-off resist perfectly perpendicularly. With small openings, more indium ends in the middle of the opening, resulting in tapered top. With larger openings, the indium entering the opening at an angle, still has more space to reach the bump edge instead of attaching to the resist wall. Deviation between the heights within a single pair is observed, especially with 6 µm and 12 µm bumps. On (a), bumps on the right are slightly smaller than on the left, which might result in problems while flip-chip bonding, as the load is not split uniformly. This deviation can be a result from a slight tilting of the wafer in the evaporator. Scanning electron micrographs of bump pairs with a diameter of 20 µm are shown in Fig. 18. Images show good profiles in the edges and surface of the bumps. Some nicks are observed, which most likely originate from the lift-off process.

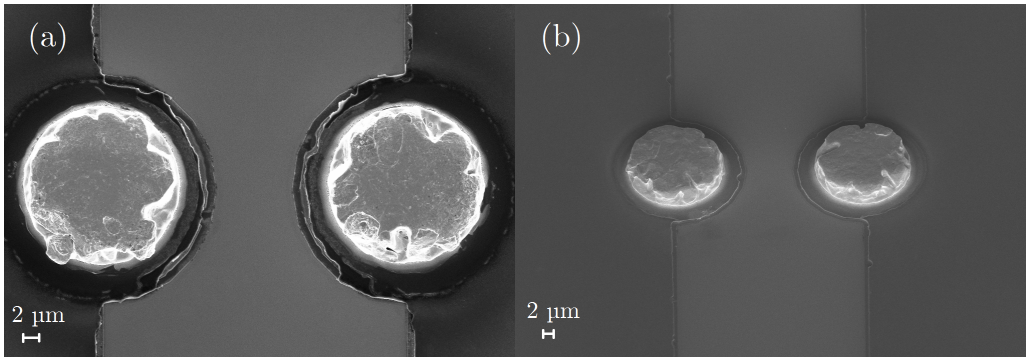

Figure 18: Scanning electron micrographs for a bump pair with a diameter of 20 µm (a): directly from top and (b): tilted view.

Fabrication of the substrates and top-chips being a wafer scale process, film thickness of the evaporated indium is a good process feedback. The measured bump height after lift-off is shown in Fig. 19. Target thickness is 3.5 µm, but a variation from 5 µm to 3.2 µm is seen. Thickest part is the middle of the wafer, and the thickness decreases regularly towards the wafer's edges. The bump diameters are 20 µm in the given data.

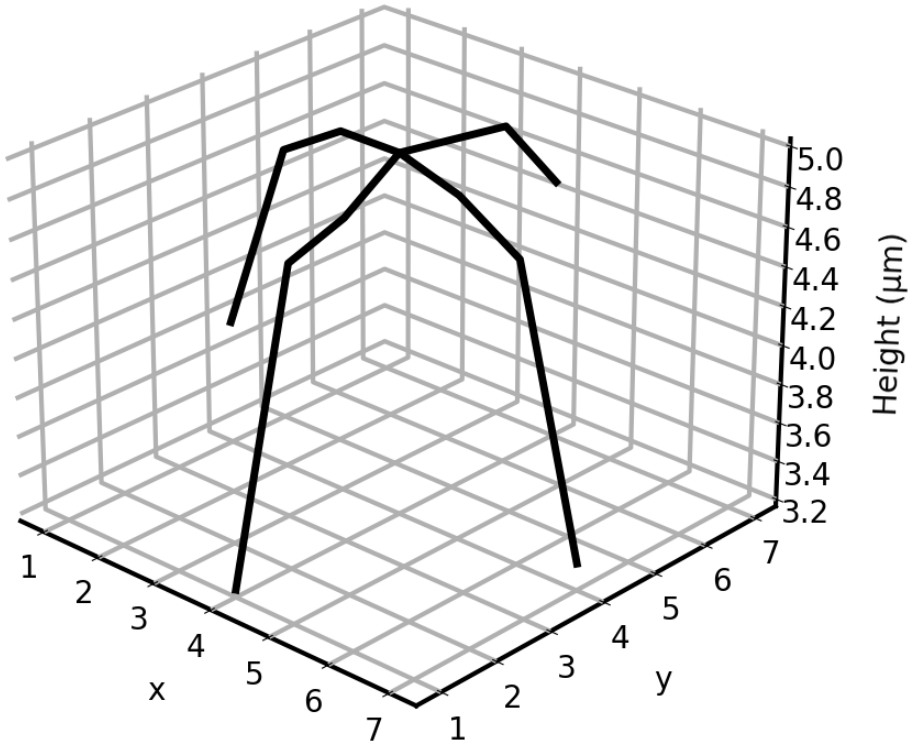

Figure 19: Bump heights in different parts of a 150 mm diameter wafer. The wafer is divided in a 7x7 grid by X and Y coordinates. Bump diameter is 20 µm.

4.1.2 Post bonding

Investigating substrates and top-chips from failed flip-chip bondings, two different failure symptoms are identified. In Fig. 20 is shown (a): SEM images and (b): 3D profile of over-squeezed and ragged bumps. In (a), top image shows the 1D series with three bump pairs. All pairs are electrically shorted from adjacent bumps touching each other. From left to right, pairs are spread more and the lower SEM image shows the rightmost pair up close. Total merging of the bumps and craters are observed. 3D profile in (b) shows example of partly merged pair where indium is removed from parts of the bumps. The over-squeezing can be explained by bad calibration or levelling of the flip-chip bonder. If the substrate and the top-chip are not levelled with high precision, bonding force is not applied uniformly to all the bumps. Tilting of the top-chip could create the result shown in Fig. 20(a). As the top-chip is not parallel to the substrate, the bumps on one edge are compressed more than on the another edge. Another possible explanation is the increasing bump height towards the edges of the wafer. However this is not observed, but the opposite, as seen in Fig. 19.

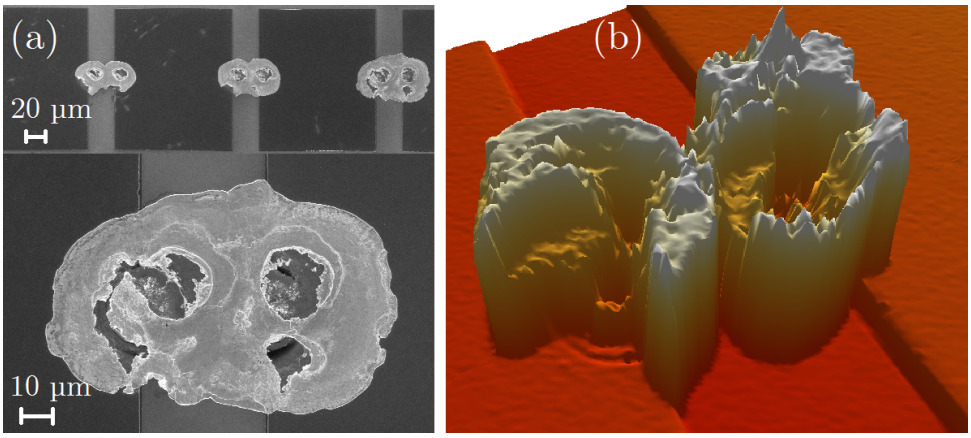

Figure 20: Scanning electron micrographs (a) and 3D optical profilometer image (b) of the bumps after faulty bonding. The bumps are compressed more towards the edge (right) of the 1D series, resulting in electrical shorts.

A second type of bond failure is depicted in Fig. 21 with a reconstructed flip-chip cross-section profile in (a) and 3D profiles of the top-chip and substrate bump pairs. The reconstructed cross-section profile is produced by measuring the bump pairs separately and combining the data to show how the flip-chip assembly has looked like. The top-chip bumps are only 0.7 µm in height after bonding, and 2.6 µm on the substrate. Neither of the chips were measured prior to bonding, but the wafer level investigation suggests the lower limit for bumps being around 3 µm. Based on this, the top-chip bumps have squeezed intensively. In the reconstructed cross-section (a), a perfect fitting of the top-chip bumps to the substrate bumps' craters is observed.

This suggests that the smaller top-chip bumps have penetrated the substrate bumps and deformed possibly from tapered profile to more flat and smoother profile. Similar faulty bonds are not observed with bumps having similar diameters and heights in both top-chip and substrate.

Improvements for the bonding process include, in addition of using similar diameters and heights in both parts of the flip-chip, removal of the native oxide from the indium bumps before bonding and higher bonding temperature. Acids such as hydrochloric acid (HCl) or hydrofluoric acid (HF) could be used to etch the native oxide of 8-10 nm just before bonding [34]. In this thesis the bonding is performed at 29 °C, but in principle the bonding temperature can be increased all the way near the melting point of indium. Initial testing with bonding temperature values of 50 °C and 100 °C are identified to be successful, but more analysis will need to be made.

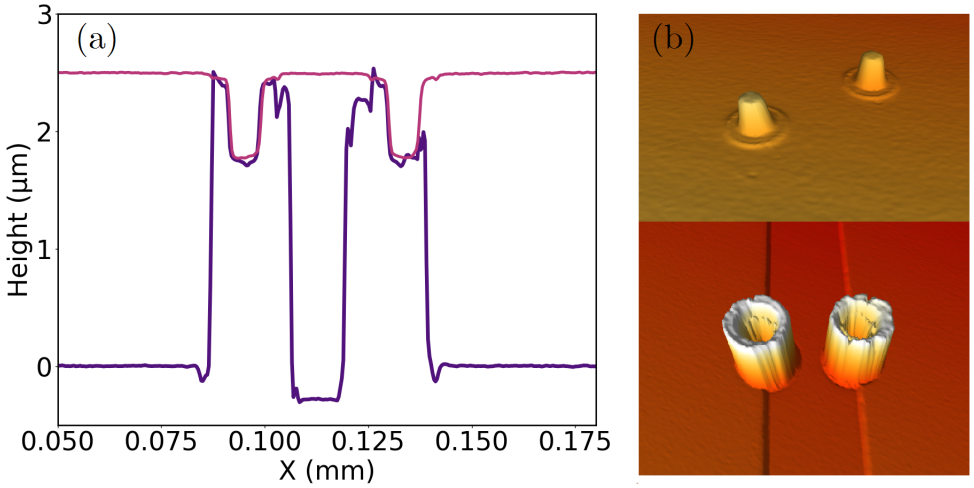

Figure 21: Reconstructed profile of a flip-chip profile (a) and 3D profiles of bump pairs (b).

4.1.3 Isolation etch

As discussed in Sect. 3.1.2, DRIE etching is critical to isolate separate top-chip islands from each other. Figure 22 shows SEM images of (a,b): flawed isolation etch, (c): top-view of separated top-chip islands and (d): cross-section of successful isolation etch. In (a) and (b), depth of the etching is 30 µm instead of minimum 40 µm required to fully penetrate the top conductive layer of silicon. Shorting of the top-chip islands causes problems in biasing the sample. A four-wire measurement scheme is shown in Fig. 23, where the solid yellow line depicts the current path with flawed isolation etching, and the dashed line depicts the designed current path. Only two tunnel junctions can be used with single bias, instead of the whole designed series, and the long silicon part leaves relatively larger series resistance compared to the junction resistances in case of flawed isolation etching. In the case of successful isolation etching, the series resistance from the silicon would not change, but more junctions would be included in the series. Simply put, less junctions means less

cooling power and larger series resistance means higher Joule heating. With an adjusted recipe the isolation etching is successful in (c), where the adjacent islands are separated from each other and (d) confirms the case with the depth of over 100 µm, exceeding the isolating oxide layer at 40 µm clearly.

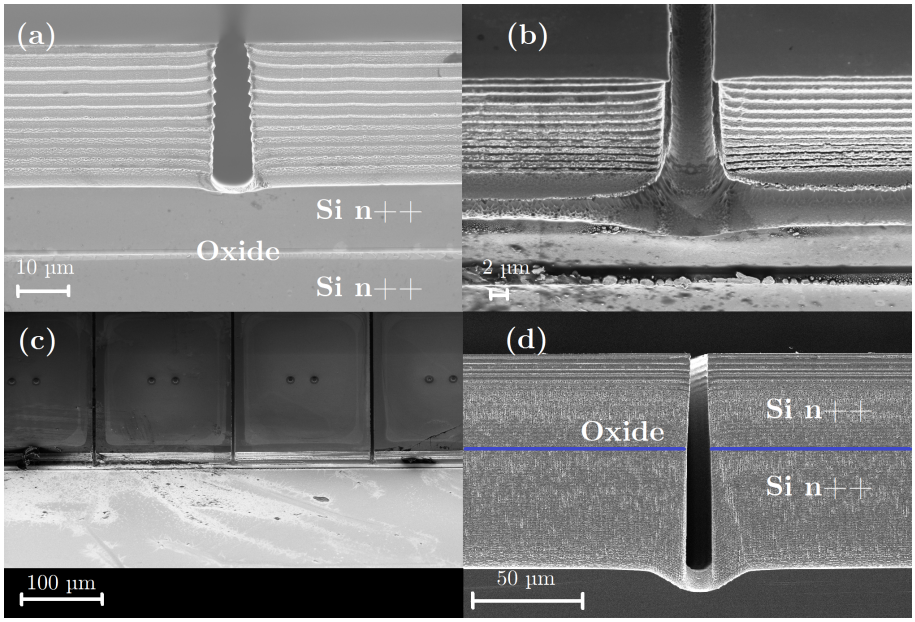

Figure 22: Scanning electron micrographs from the top-chip isolation etch investigation. (a) and (b): Flawed isolation etching with shallow trenches of 30 µm. (c): Top-view of the top-chip island chain. (d): Successful isolation etch of 100 µm.

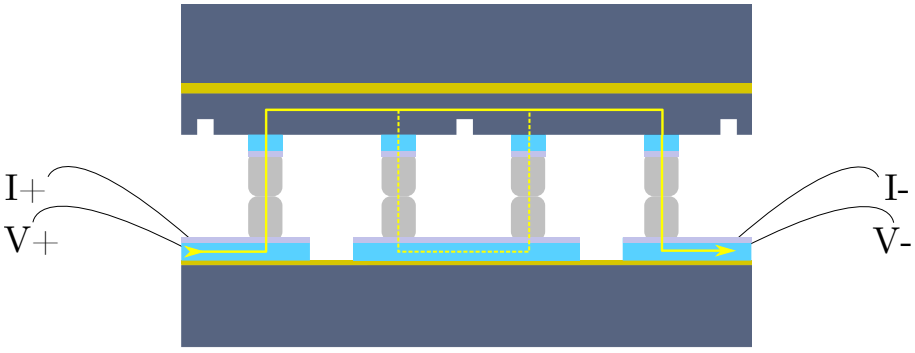

Figure 23: Current flow with flawed isolation etching (solid line) and with designed etching (dashed line).

4.2 Thermal resistance

The flip-chip sample consist of a substrate having 200 nm Al + 50 nm Ti layer below the indium bumps. The Al layer functions as a intermediate conduction layer. The Ti layer serves as an adhesion surface for the indium bumps. Top-chip has 500 nm Al layer within oxide layer between Al and silicon, which serves as a tunnel barrier. Top-chip also has a 25 nm Ti layer as an adhesion layer. The junction or barrier has circular cross-section with 6 µm diameter. Indium bumps' diameters are 20 µm and 18 µm for the substrate and the top-chip, respectively. The sample parameters are collected in Tab. 1.

	S3	C3
Stack (nm)	Al 200 + Ti 25	Al 500 + Ti 25
Bump diameter (µm)	20	18
Bump height (µm)	3-5	3-5
Barrier diameter (µm)	-	6

Table 1: Sample parameters for the substrate and the top-chip.

The IV characteristics for the thermometer SINIS and the heater SINIS are measured with the setup presented in Sect. 3.3.1 are shown in Fig. 24. A theoretical model is fitted for both of the devices separately. The model consists of two NIS junctions and a series resistance from silicon:

$$V_{\text{bias}} = V_1(I_1, R_{\text{T},1}, T_t, T_{\text{C}}, V_{\text{offs, t}}, \gamma_1) + V_2(I_2, R_{\text{T},2}, T_t, T_{\text{C}}, V_{\text{offs, t}}, \gamma_2) + R_{\text{Si}} I \quad (25)$$

$$I = I_1 = I_2 \quad (26)$$

where V_{bias} is the measured voltage over the device, $V_{1(2)}$ is the voltage over a single junction solved from $I_{1(2)}$ (Eq. 9), R_{Si} is the series resistance from the silicon between the junctions and I is the current through the series resistance. Equation 26 is the current conservation, the same current flows through the junctions and the series resistance. The fitting parameters in the tunnel junction equations are, in addition to the current, the tunneling resistance $R_{\text{T},1(2)}$, temperature of the normal metal and the superconductor T_t, critical temperature of superconductor T_{C}, voltage offset caused by the measurement setup $V_{\text{offs,t}}$ and the Dynes parameter $\gamma_{1(2)}$. Subscripts 1,2 imply the junction number and subscript t is the bath temperature (cryostat temperature) the data is measured. For simplicity, the electron temperature of the normal metal and the superconductor are set equal, but independent from the bath temperature, thus $T_{\text{N}} = T_{\text{S}} = T_t \neq T_{\text{bath}}$. The approximation is justified with bias voltages near zero $V_{\text{bias}} \simeq 0$, where self-heating or cooling is negligible. In addition, with large bias voltages $V_{\text{bias}} \gg \Delta/e$ the device is likely to be overheated, which does not show because the bias energy eV is much larger than the thermal energy $k_{\text{b}}T_{\text{N(S)}}$, $eV \gg k_{\text{b}}T_{\text{N/S}}$. The model is insufficient for describing $T_{\text{N}} \neq T_{\text{S}}$ behaviour within the energy gap, but gives estimates for R_{T}, γ, T_{C} and R_{Si}. The insets in Fig. 24 show the discrepancy between the data and the model in the gap region.

The IV data is presented for three bath temperature values: 8 mK, 150 mK and 400 mK. The fit parameters including the standard errors (68% error bar) are summarized in Tab. 2. Based on the fits, both devices have symmetric junctions with equal tunneling resistances within the junctions. The result is anticipated as the junctions were fabricated with the same process. Fit temperature values differ from the given bath temperatures. At 8 mK bath temperature, the thermometer and the heater are 60 mK and 67 mK, respectively. At 150 mK the values are 128 mK and 120 mK, and at 400 mK they are 373 mK and 370 mK. The values at 150 mK and 400 mK bath temperature values can be explained by the error in the cryostat's thermometer's calibration. At 8 mK, the relative discrepancy is 650 %. One possible explanation, in addition to the calibration, is the self-heating of the sample combined with insufficient thermalization to the bath. The critical temperature values T_C of the superconductors are 1.15 K for all heater and thermometer junctions, which is effectively the critical temperature of film aluminum, corresponding to $\Delta_0 = 175$ µeV by Eq. 4. Series resistance is found to be non-negligible, 4.1 Ω for both devices. Geometry of the series resistance is expected to be equal in both devices, thus the equal values are not surprising. The Dynes parameters are in line with low resistance Si-Al junctions. Scaling the tunneling resistance with the barrier area gives the characteristic tunneling resistances of 1.35 kΩµm^2 and 0.5 kΩµm^2 for the thermometer and heater, respectively.

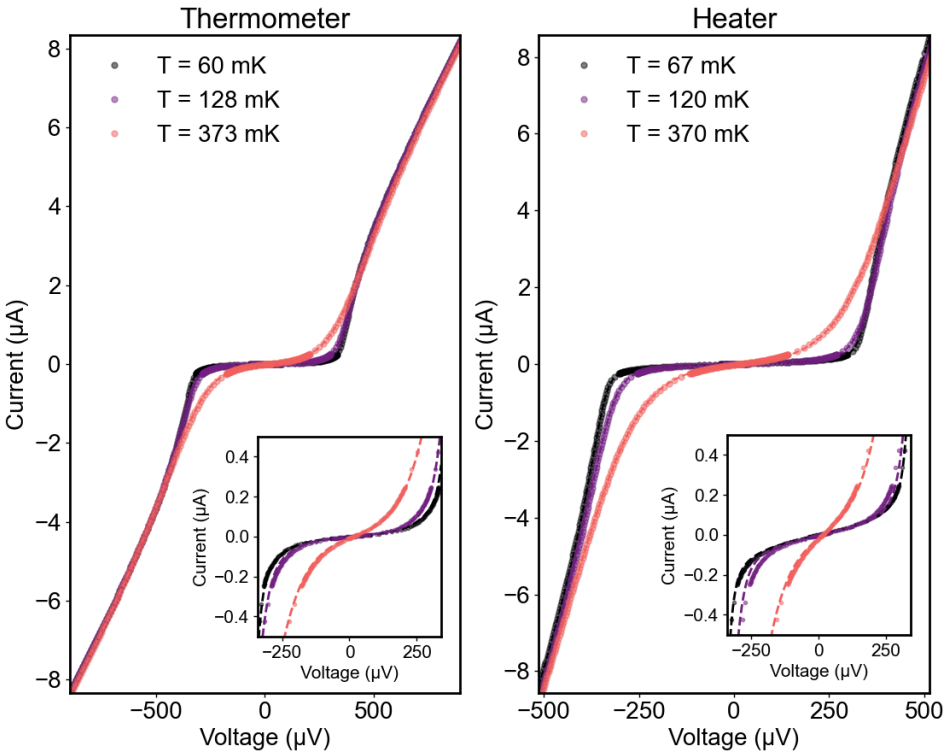

Figure 24: IV characteristics of the thermometer and the heater. The temperature values are fitted model parameters. The insets highlight the discrepancy between the data and the model in the gap region.

	Thermometer	Heater
$R_{\mathrm{T},1}$ (Ω)	47.7 ± 1	18.9 ± 1
$R_{\mathrm{T},2}$ (Ω)	47.7 ± 3	18.9 ± 0.2
T_8 (mK)	60 ± 1	67 ± 5
T_{150} (mK)	128 ± 1	120 ± 6
T_{400} (mK)	373 ± 12	370 ± 8
T_{C} (K)	1.15 ± 1e-4	1.15 ± 1e-3
R_{Si} (Ω)	4.1 ± 0.2	4.1 ± 0.9
γ_1	7.3e-3 ± 6e-4	1.5e-2 ± 9e-4
γ_2	3.5e-2 ± 8e-4	1.0e-2 ± 4e-4

Table 2: Obtained model parameters for the thermometer and the heater for S3C3 flip-chip. Subscripts 8, 150 and 400 imply bath temperature in milliKelvins and superscripts 1 and 2 imply different NIS junctions in the SINIS stack.

Utilizing the fitted model parameters from Tab. 2, the thermometer's voltage response as a function of the electron temperature in the normal metal is modeled in Fig. 25. The model is compared to the measured zero bias voltage as a function of the bath temperature. The model corresponds better to the measured data at $T_{\mathrm{bath}} \geq 150$ mK compared to the values with $T_{\mathrm{bath}} < 150$ mK. At the lower temperature values, the model starts to underestimate the voltage measured, which has at least two possible reasons. The model can underestimate the Dynes parameters, resulting in smaller subgap resistance thus smaller voltage response at low temperature. Secondly, the measurement scheme introduced in Sect. 3.3.2 assumes galvanic isolation between the thermometer and the heater, which is not the case with the sample discussed. The problem is countered by current biasing both devices and using AC coupling for the thermometer, but the DC bias could leak from the heater to the thermometer and cause shift in the operation point, away from the zero bias. Non-zero operation point would directly change the voltage response and increased bias generates more Joule heating. In the current device design, thermometer's junctions are fabricated identically with other junctions in the device. Ideally, the resistance in the thermometer should be high as possible, to reduce self-heating. However, the fabrication process had to the kept simple enough, but needs to be improved in the following designs. Motivated by the low temperature anomaly, the temperature data with $T_{\mathrm{bath}} < 150$ mK is disregarded from the analysis. Thermometer's AC current bias is 0.5 nA at frequency of 18 Hz.

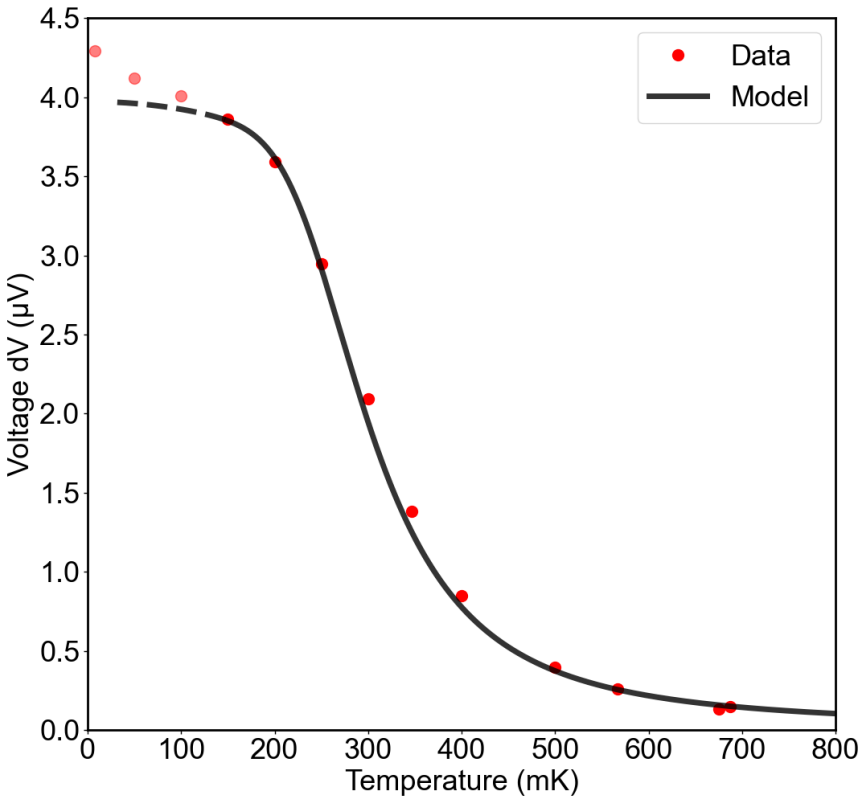

Figure 25: Measured zero bias AC voltage as a function of bath temperature and the model curve based on the parameters extracted from the IV fits. Data at low temperature values $T_{\mathrm{bath}} < 150$ mK differ from the model and they are not used in the analysis. Current bias for the thermometer is 0.5 nA.

Two examples of the measured temperature difference as a function of the heating power, which is a sum of heating from both junctions as given in Eq. 12 and Joule heating in the series resistance given by Eq. 20 are shown in Fig. 26. The temperature difference δT is between the bath temperature implied in the legends, and the sample temperature given by the measured AC voltage and the thermometer calibration. Linear models are fitted to the data at relatively low temperature differences from 7 mK to 20 mK, as the approximation in Eq. 18 holds only for the low temperature differences compared to the operation temperature. Thermal interface resistance is calculated with Eq. 21, using the total contact area in the flip-chip assembly. The result is given in Fig. 27 and compared to the result by Mykkänen *et al.* in [9]. The given result is around ten times higher than in the reference, with $T^{-2.7}$ temperature dependence, whereas the reference has T^{-3} temperature dependence. The error bars in the data are dominated by the model parameter errors. Dashed

lines represent the 95% confidence intervals. Data with bath temperature of $T > 150$ mK is additionally restricted to $T_{\mathrm{bath}} \leq 400$ mK motivated by thermal noise present in higher-temperature data, which drastically increases the fit uncertainties. Even though the measured temperature range is narrow, the conclusion is clear. The 3D integration through the flip-chip design and bonding increases the thermal interface resistance, which is a large factor in optimizing the cooler performance. Increased Kapitza resistance directly reduces the heat leak from the overheated superconductor to the cooled normal metal.

In Ref. [9], the cooled normal metal part is suspended from the bath by superconducting leads and the tunnel junctions are formed on the contacts between the normal metal island and the leads. The thermal design is relatively similar to the one studied in this thesis. Here the normal metal island is suspended by flip-chip bonding and the superconducting leads are replaced by indium bumps. The order of magnitude difference in the thermal resistance is a significant improvement, which can result from several differences. Starting from the possibly overheated superconductor, the studied design has a total of five different interfaces (Al-Ti-In-Ti-Al-Si n++) which affect the thermal transport from the substrate to the top-chip, in contrast to only one in the reference (Al-Si n++). However, studying this dependence is out of scope of the thesis. The thermal gradient forming between the subsystems is also not trivial with different materials, and needs a thorough investigation in further development of the flip-chip microcooler.

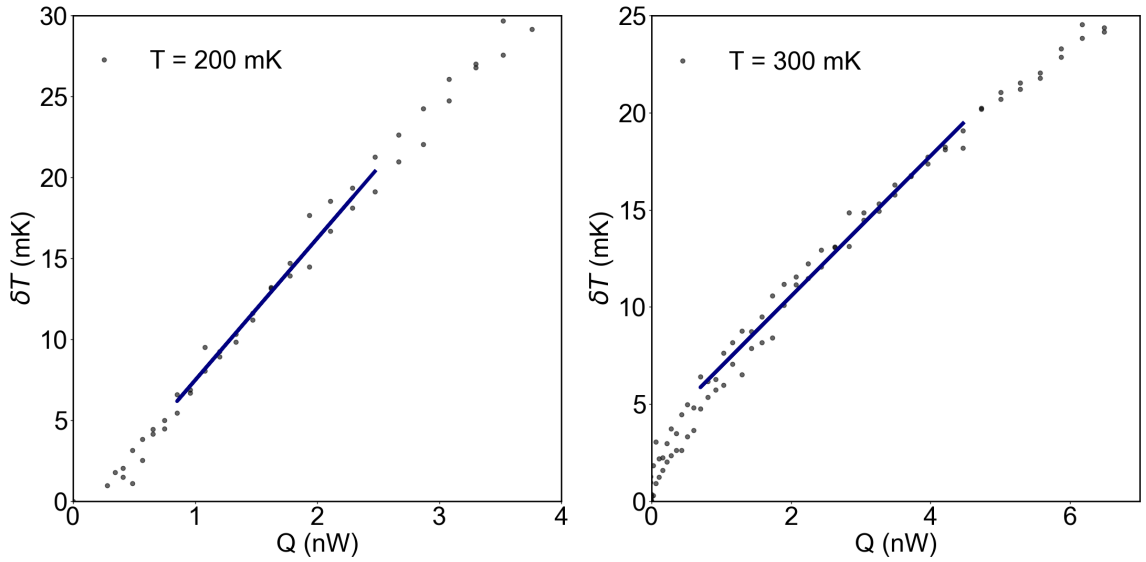

Figure 26: Temperature difference of the sample relative to the bath temperature as a function of heating power at (a): 200 mK and (b): 300 mK. Linear fits from $\delta T =$ 7 mK to 20 mK are used to extract the thermal resistance at each temperature.

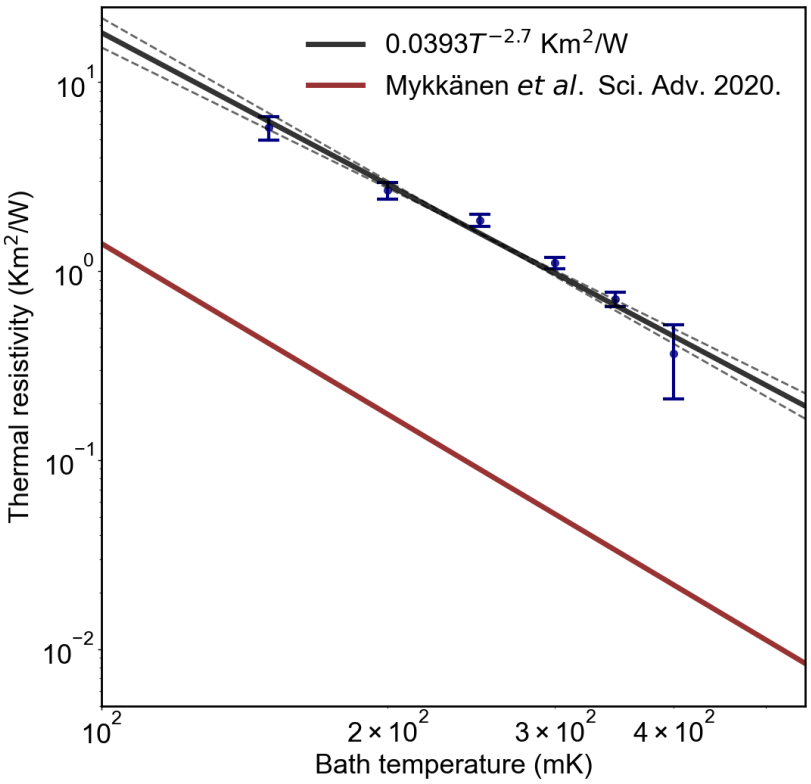

Figure 27: Calculated Kapitza resistance as a function of temperature with $T^{-2.7}$ relation compared to the result from [9].

5 Summary and future prospects

In this thesis, vertical integration of superconducting solid state coolers was studied by utilizing a flip-chip bonding technique for interconnecting a substrate and a top-chip. The top-chip contains the tunnel junctions and the substrate forms series connections between the junctions. Essential background was given on superconducting tunnel junctions and flip-chip bonding. Experimental methods were discussed, including the fabrication and the measurement side.

The quality assurance showed non-uniform bump height distribution and diameter dependent height profiles for indium bumps. Bumps with larger diameter (20 and 25 µm) were observed to be mostly uniform in quality. Detached flip-chips were investigated and two failure mechanisms were identified. Over-squeezed bumps were pointed towards bad calibration in the bonder, flawed levelling of the substrate and the top-chip, or uneven bump heights. Second failure type was more subtle, where the small top-chip bumps had created smooth craters on the larger substrate bumps, and detached. As a conclusion, one should use similar bumps in diameter and height at both parts of the flip-chip. The isolation etching was shown to be too shallow, not galvanically isolating the adjacent top-chip islands. Adjusted recipe was confirmed to be successful. Thermal resistance measurements were conducted for the flip-chip sample with flawed isolation etching, and the thermal interface resistance was found to be ten times higher than in the previous work [9] The result shows that the flip-chip method can provide 3D integration, tied with increased thermal interface resistance, which is essential for coolers operating at hundreds of milliKelvins.

Future prospects of a vertically integrated cooler is to demonstrate electronic cooling. After that, a lot can be optimized in the process. At the moment the overheating of the superconductors has not been addressed, as the stack has no quasiparticle traps. Introducing traps to the device design could reduce the heat load from the quasiparticle backflow. Additionally, the bumps could be fabricated with electroplating, which is more suitable for growing several micrometer thick metal layers. In the current design, all the junctions are fabricated to be equal within the device. In the future, high resistance thermometers will be introduced to reduce the self-heating by utilizing smaller currents needed for sufficient voltage response. Ultimate target would be a multi-stage, cascaded 3D integrated cooler, able to cooldown from a pulse tube compatible temperature to milliKelvins, offering a compact alternative to dilution-based cooling mechanisms. To cover this temperature range from around 3 K to 10 mK, multiple cooler stages with different critical temperatures are required. An example of this development is in the work submitted as the special assignment in 2019 by the author of this thesis, where transparent vanadium-silicon junctions are investigated. Additionally, the data is presented in the preprint [14] pending for review.

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